STM32 Seminar

Peripherals

Agenda

- 09:00 Registration
- 09:30 Introduction to ST
- 09:40 STM32 Overview
- 09:45 ARM – an introduction to Cortex-M3
- 10:30 STM32 Cortex-M3 Core and System
- 11:30 Coffee

- 11:45 Hitex – Tools, DMA, RTOS
- 12:45 Lunch

- 13:30 STM32 Peripherals
- 15:00 Coffee
- 15:15 STM32 Libraries examples and Usage
- 15:45 STM32-Primer demo
- 16:15 Summary, Questions, and Close

Agenda

- 09:00 Registration
- 09:30 Introduction to ST
- 09:40 STM32 Overview
- 09:45 ARM – an introduction to Cortex-M3
- 10:30 STM32 Cortex-M3 Core and System
- 11:30 Coffee

- 11:45 Keil Tools
- 12:45 Lunch

- 13:30 **STM32 Peripherals**
- 15:00 Coffee
- 15:15 STM32 Libraries examples and Usage
- 15:45 STM32-Primer demo
- 16:15 Summary, Questions, and Close

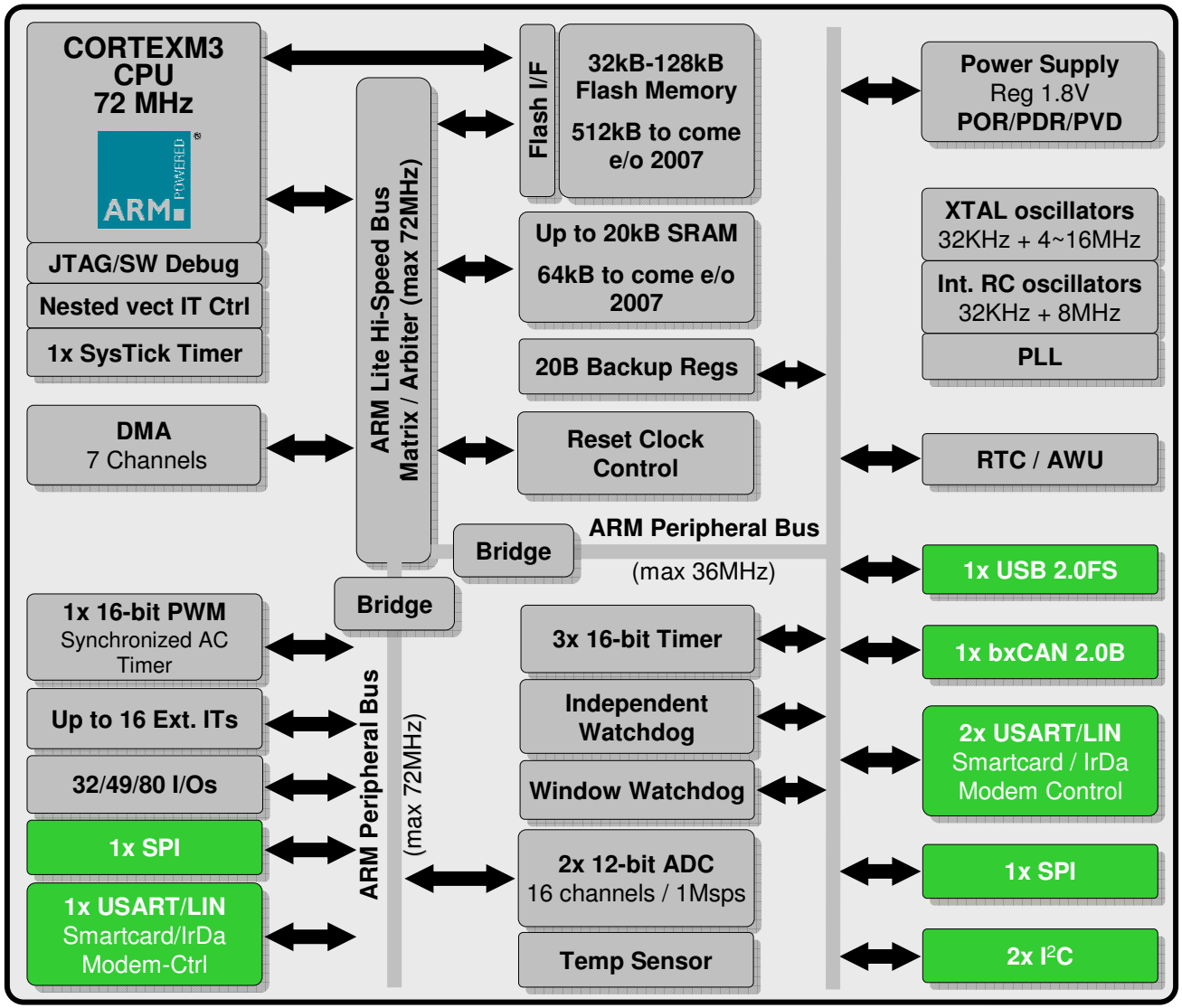
STM32 Peripherals

- Communications Peripherals
- Analog to Digital Converter
- Timers
- Demo: USB Device Firmware Upgrade

STM32 Communication Peripherals

STM32F10x Series Block Diagram

- Nine Communications Peripherals:
  - 2 x SPI
  - 2 x I2C
  - 3 x USART
  - CAN2.0B
  - USB 2.0 Full Speed

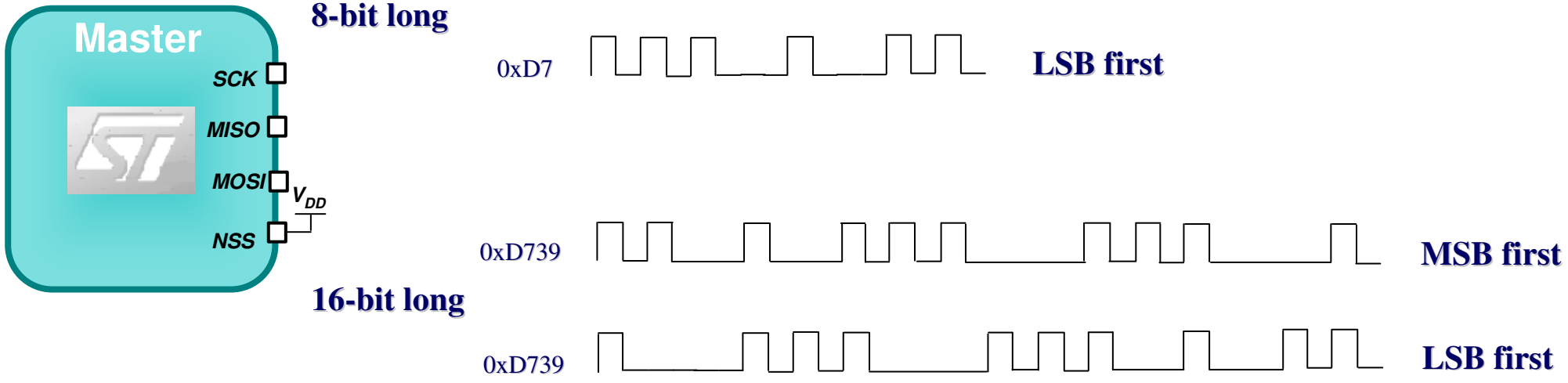


SPI Serial Peripheral Interface

- Two SPIs: SPI1 on high speed APB2 and SPI2 on low speed APB1
- Up to 18 MHz data rate in either Master or Slave modes
- Full duplex and simplex synchronous transfers supported
- Programmable data frame size: 8/16-bit transfer frame format selection
- Programmable data order: MSB-first or LSB-first shifting
- Programmable clock polarity & phase
- Hardware or software nSS management
- Interrupt/DMA request generation:
  - Tx Buffer Empty, Rx Buffer Not Empty, Bus Fault, Overrun
- Hardware CRC support: CRC8 / CRC16-CCITT standard

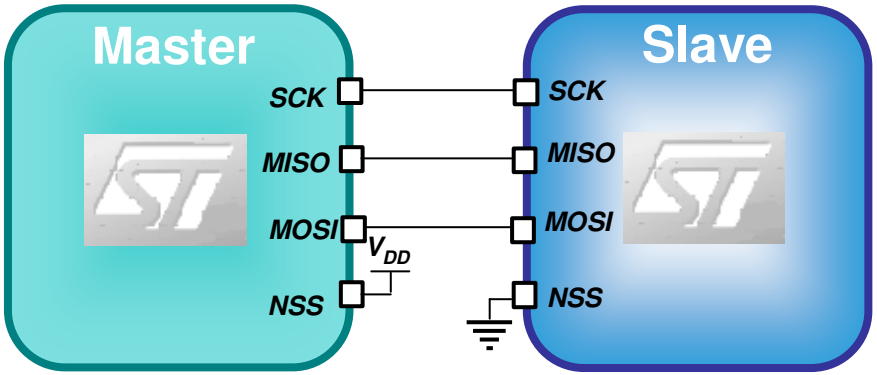
SPI Data Frame Format

- Programmable data frame size: 8 or 16-bit frame format
- Programmable data order: MSB or LSB-first



SPI Full Duplex Communication

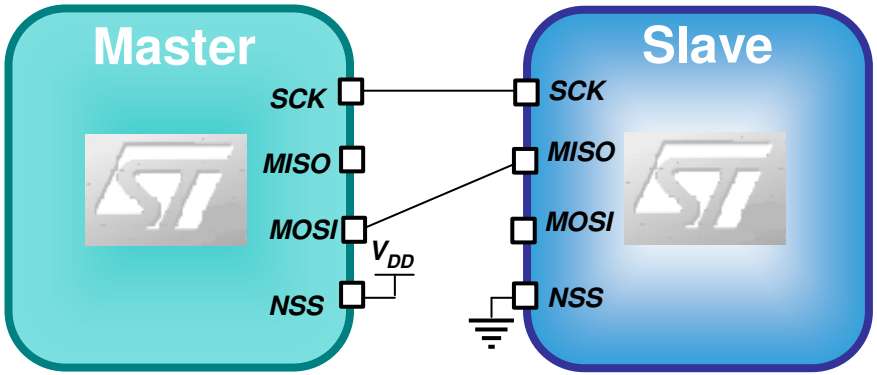
- Standard full duplex 3-wire transfer



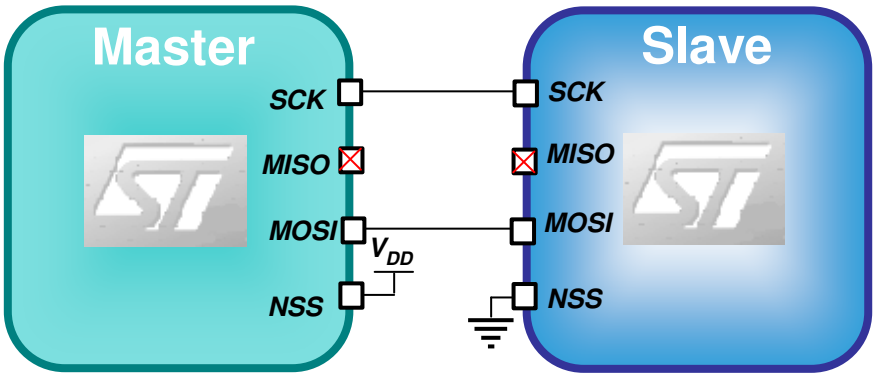
Full Duplex

SPI Simplex Communication

- Simplex modes for pin saving
- Bi-directional: two wire, direction control bit
- Slave Rx-Only: two wire, uni-directional



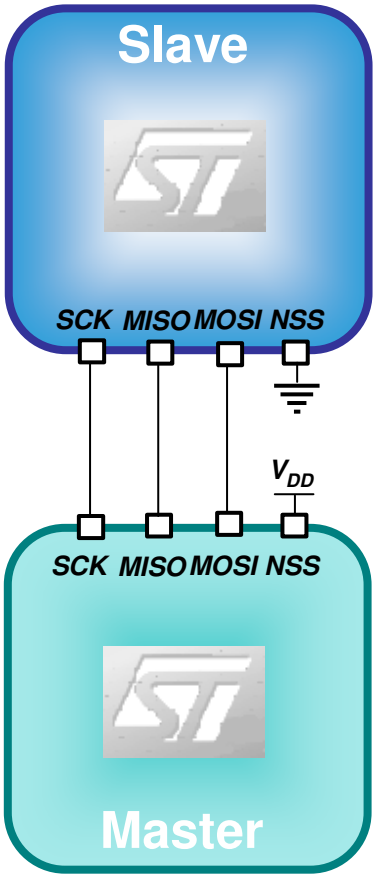
Bi-directional



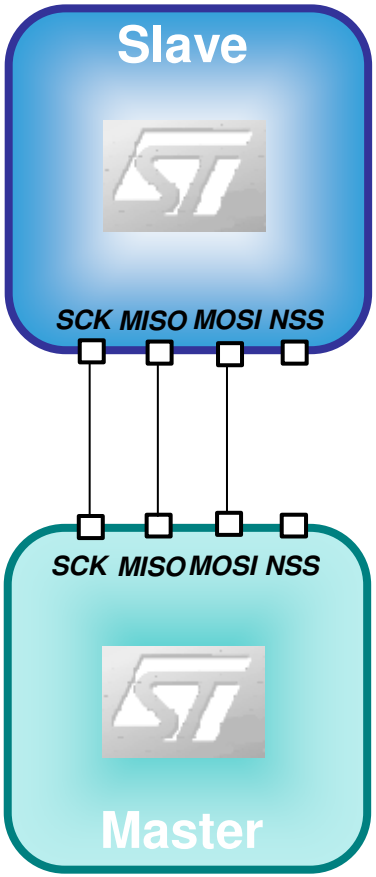
Rx Only (Slave)

SPI NSS Hardware & Software Management

Hardware NSS

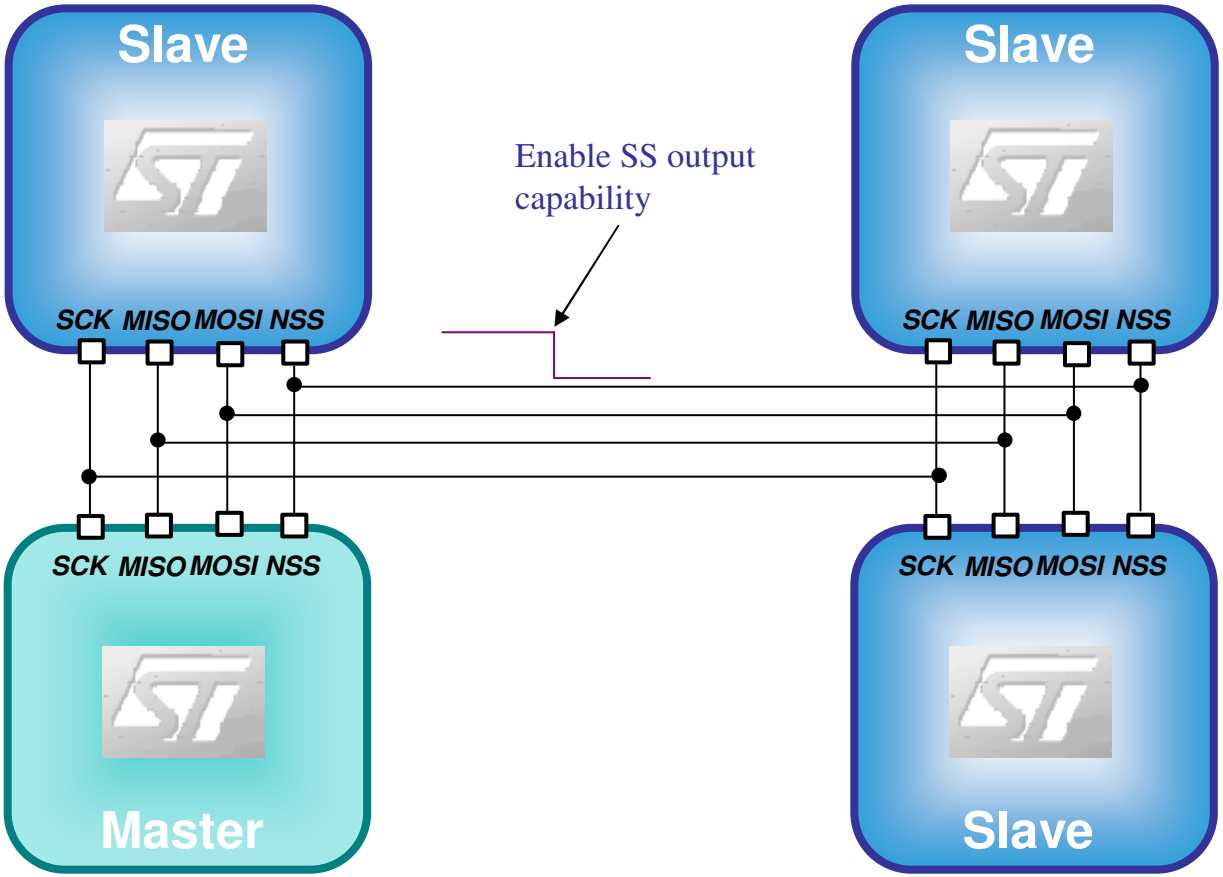


Software NSS



- Full Duplex pin saving mode
- Frees Master and Slave NSS pins
- Dynamic Master/Slave re-configuration

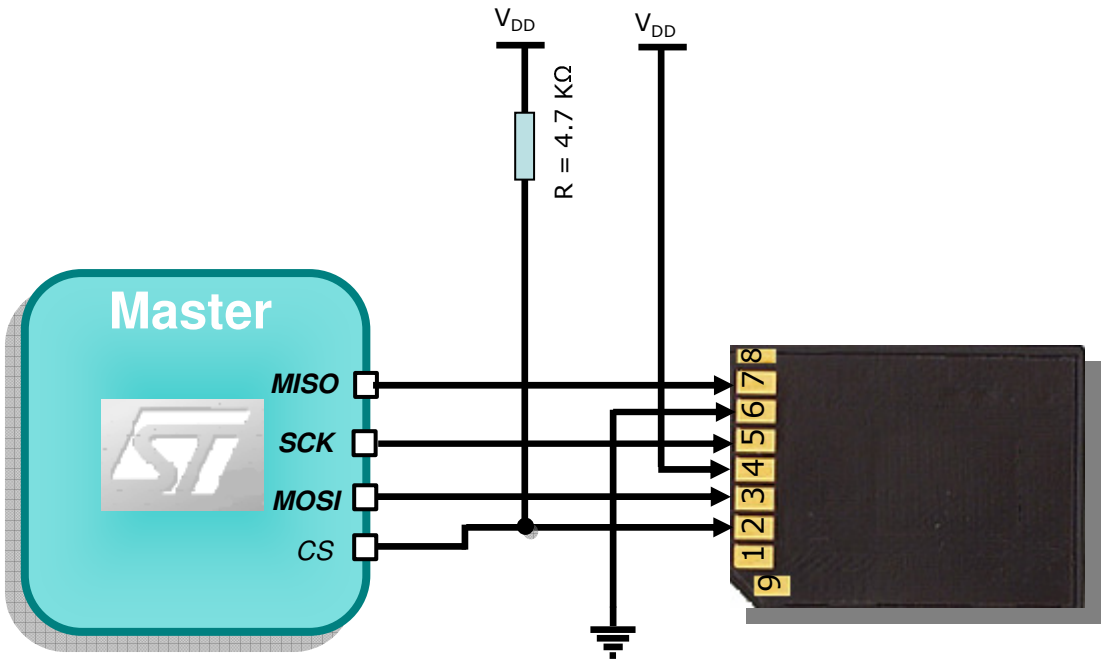
SPI Single Master: SS Output Management



- Each device can be a unique master by enabling its NSS as output and driving it low: all other devices became slaves.
- No need for external GPIO pin to drive slaves NSS pins

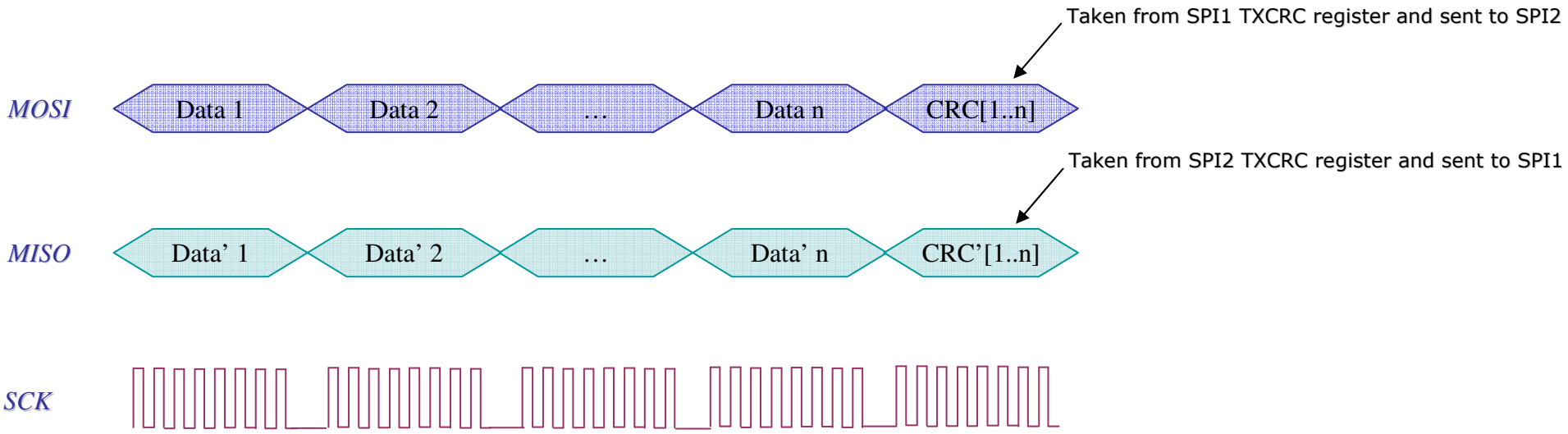
SPI SD/MMC Card Support

- Basic SD/MMC support (SPI protocol):
  - Performance: speed up to 18MHz
  - Error checking: hardware CRC calculation



SPI CRC Calculation

- Example of n data transfer between two SPIs followed by the CRC transmission of each one in Full-duplex mode



Inter Integrated Circuit (I2C)

I2C Features (1/3)

- Multi-Master and Slave capability
- Controls all I²C bus specific sequencing, protocol, arbitration and timing
- Standard and fast I²C modes (up to 400kHz)
- 7-bit and 10-bit addressing modes
- Clock stretching supported
- Dual addressing capability to acknowledge 2 slave addresses
- Configurable PEC (Packet Error Checking) Generation or Verification:
  - PEC value can be transmitted as last byte in Tx mode
  - PEC error checking for last received byte

I2C Features (2/3)

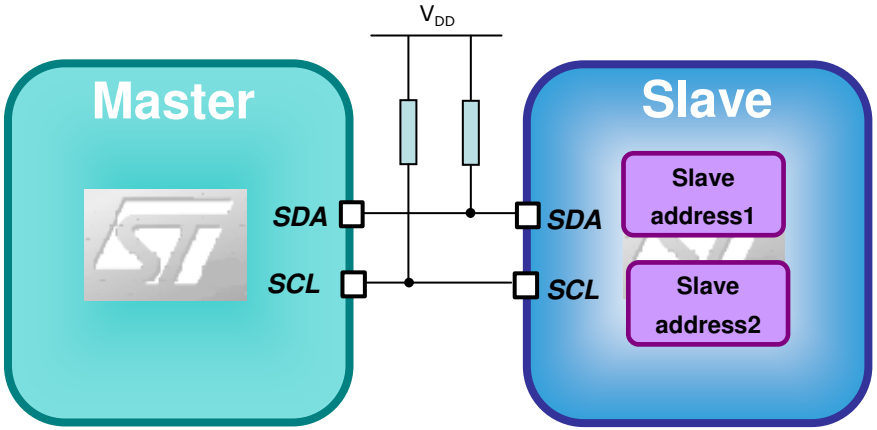
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgement failure after address/ data transmission
  - Detection of misplaced start or stop condition
  - Overrun/Underrun if clock stretching is disabled
- 2 Interrupt vectors:
  - 1 Interrupt for successful address/ data communication
  - 1 Interrupt for error condition
- SMBus 2.0 (System Management Bus) Compatibility – http://smbus.org
- PMBus™ (Power Management Bus) Compatibility – http://pmbus.org

I2C Features: DMA (3/3)

- DMA supported for TX and RX
- Requests mapped on separate DMA channels, supporting simultaneous bi-directional transfers
- Calculated PEC value is automatically transmitted at end of frame

I2C Dual Addressing Mode

- I2C supports dual addressing capability to acknowledge 2 slave addresses



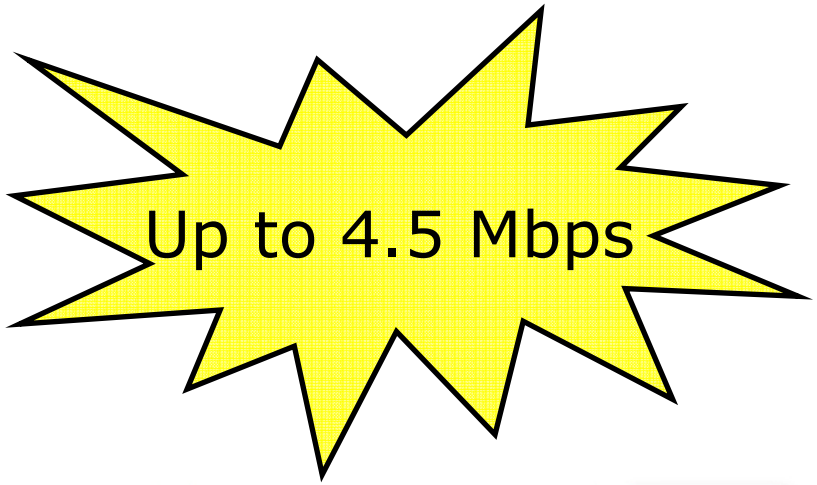
I2C SMBus Mode

- Intel System Management Bus SMBus 2.0 Compatibility
- Low cost, more robust than standard I²C
- Clock stretching support for different speed devices
- Timeout: 25ms clock low timeout delay
- H/W Packet Error Checking (PEC) with ACK control
- Address Resolution Protocol (ARP) supported
- SMBALERT# line for interrupts
- Host Notify Protocol

Universal Synchronous Asynchronous Receiver Transmitter (USART)

USART Features (1/2)

- Three USART: USART1 High speed APB2 and USART2/3 on Low speed APB1
- Fully-programmable serial interface characteristics:
  - 8 or 9 bit data
  - Even, odd or no-parity generation and detection
  - 0.5, 1, 1.5 or 2 stop bits
  - Programmable fractional baud rate generator (12-bit Integer, 4-bit Fraction)
  - Hardware flow control (CTS and RTS)
- Dedicated transmission and reception flags (TxE and RxNE) with interrupt capability
- Support for DMA
  - Receive DMA request
  - Transmit DMA request



USART Features (2/2)

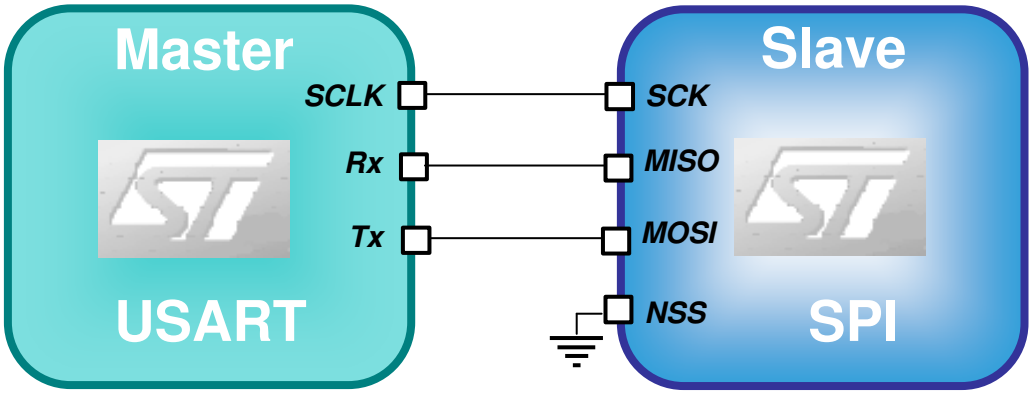
- 10 interrupt sources to ease software implementation
- LIN Master/Slave compatible
- Synchronous Mode: Master mode only
- IrDA SIR Encoder Decoder
- Smartcard Capability
- Single Wire Half Duplex Communication
- Multi-Processor communication
  - USART can enter Mute mode
  - Mute mode: disable receive interrupts until next header detected
  - Wake up from mute mode (by idle line detection or address mark detection)

USART DMA Capability

- DMA supported for TX and RX
- Requests mapped on separate DMA channels, supporting simultaneous bi-directional transfers

USART Synchronous Mode

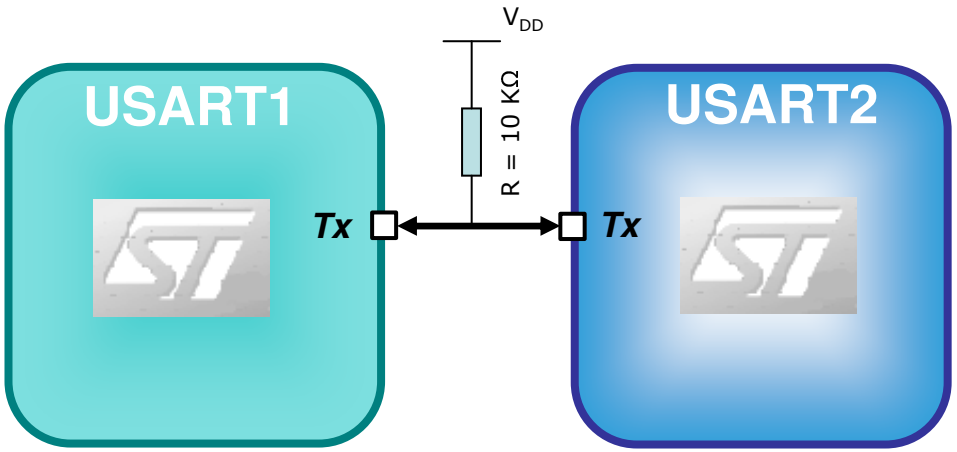
- USART supports Full duplex synchronous communication mode
  - Full-duplex, three-wire synchronous transfer
  - USART Master mode only
  - Programmable clock polarity (CPOL) and phase (CPHA)
  - Programmable Last Bit Clock generation
  - Transmitter Clock output (SCLK)



Full Duplex

USART Single Wire Half Duplex mode

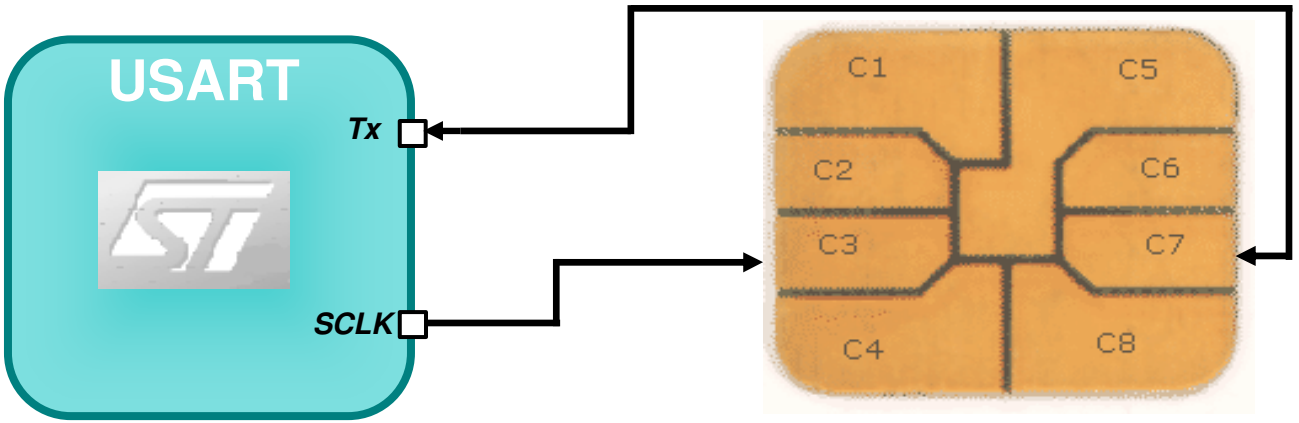
- USART supports Half duplex synchronous communication mode
  - Only Tx pin is used (Rx is no longer used)
- Used to follow a single wire Half duplex protocol.



Half Duplex

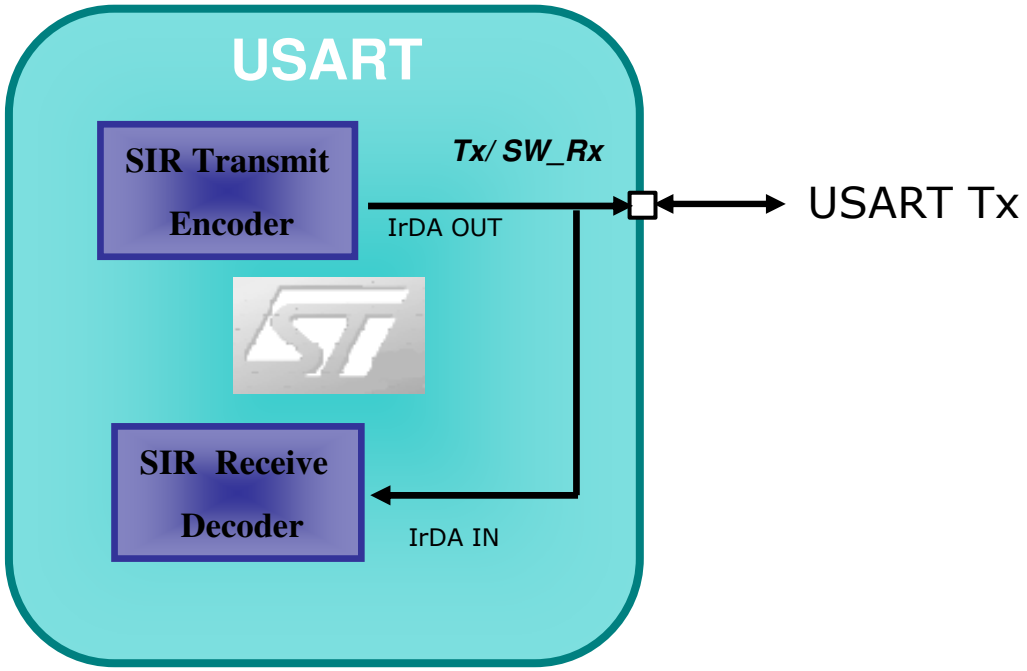
USART Smart Card mode

- USART supports Smart Card Emulation ISO 7618-3
  - Half-Duplex, Clock Output (SCLK)
  - 9Bits data, 0.5 Stop Bit in receive, 1.5 Stop Bits in transmit
  - Parity Error Generation with NACK transmission
  - Programmable Guard Time
  - Programmable Clock Prescaler to guarantee a wide range clock input



USART IrDA SIR Encoder Decoder

- USART supports the IrDA Specifications
  - Half-duplex, NRZ modulation,
  - Max bit rate 115200 bps
  - 3/16 bit duration for normal mode
  - Low power mode: 1.42MHz<USART Prescaler<2.12MHz



Half Duplex

Controller Area Network (bxCAN)

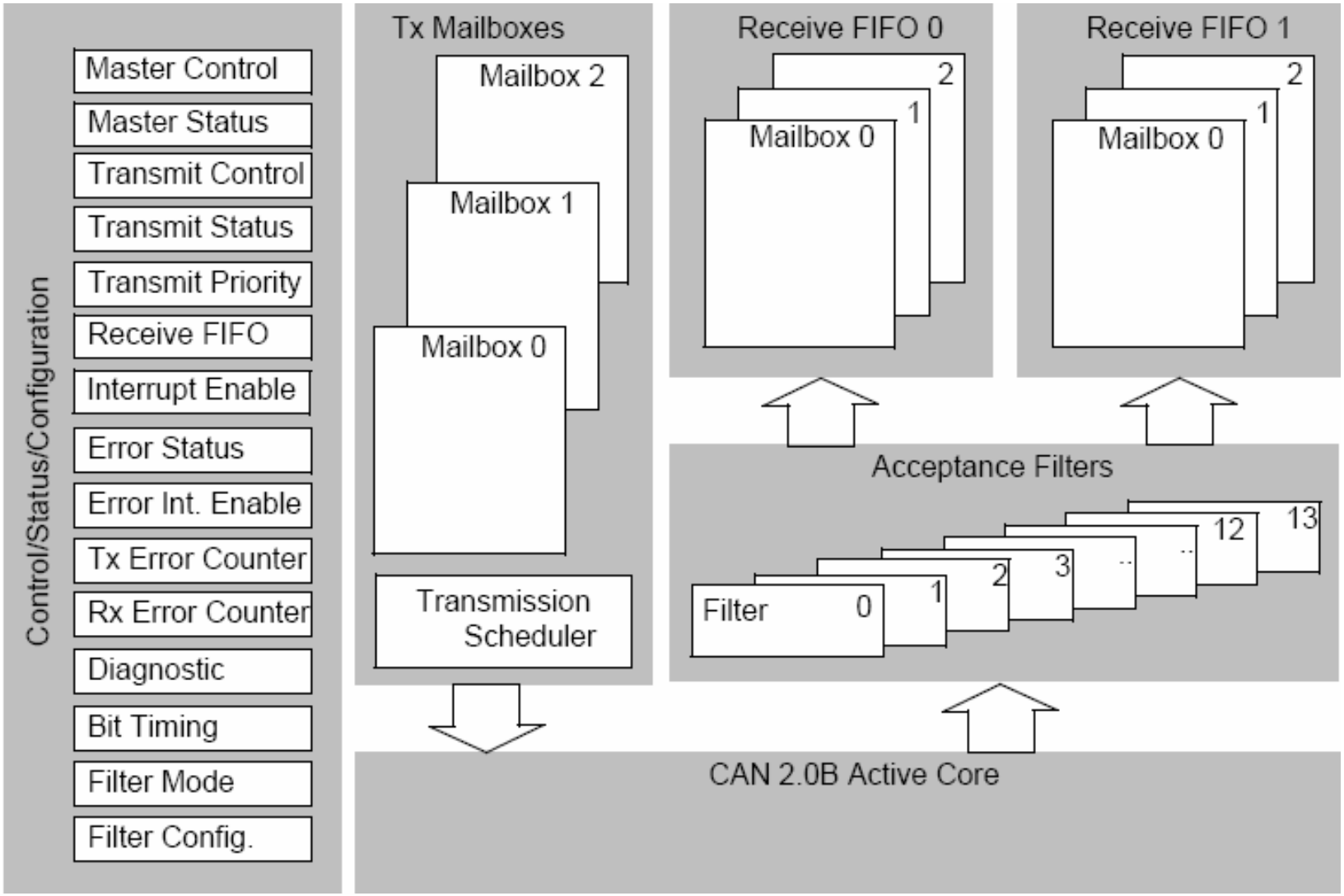
CAN Features (1/2)

- Main features:
  - Supports CAN protocol version 2.0 A, B Active
  - Bit rates up to 1Mbit/s
  - Supports Time Triggered Communication
- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
  - Time Stamp on SOF transmission
- Reception
  - Two receive FIFOs with three stages
  - 14 scalable filter banks
  - Identifier list features
  - Configurable FIFO overrun
  - Time Stamp on SOF reception

CAN Features (2/2)

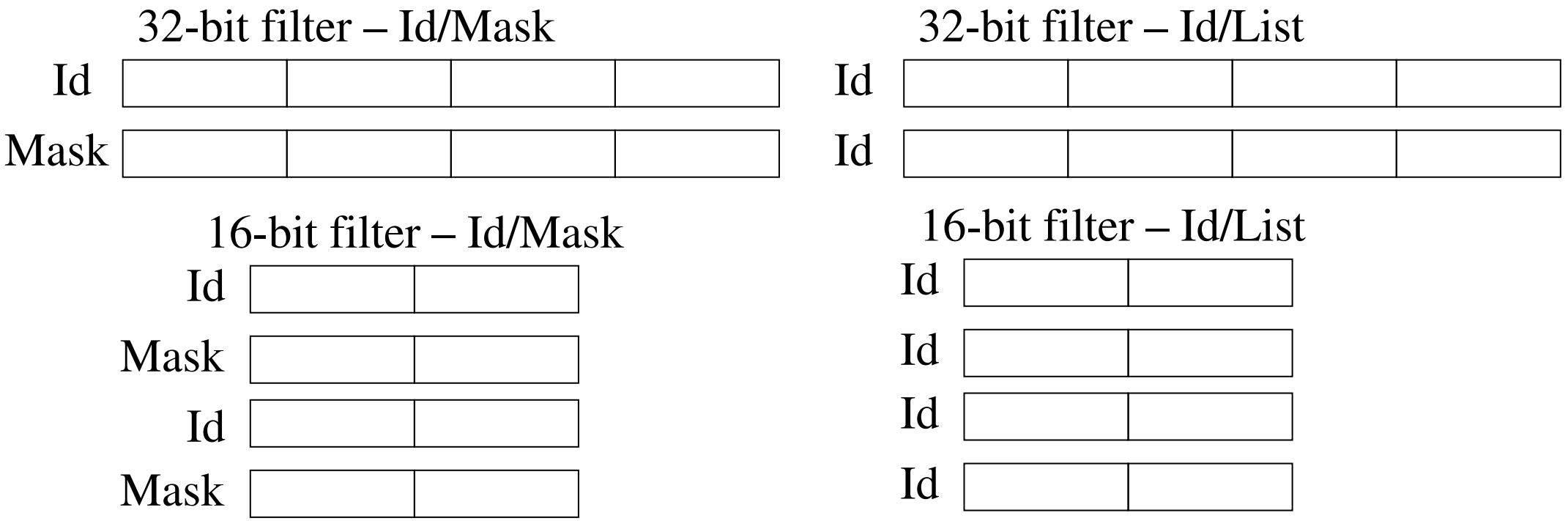
- Time Triggered Communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Configurable timer resolution
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space
  - 512 bytes reserved RAM size
  - 4 dedicated interrupt vectors: transmit interrupt, FIFO0 interrupt, FIFO1 interrupt and status change error interrupt

STM32 CAN Block Diagram



Filter Bank Scale and Mode Configuration

- Up to 14 filter banks
- Scale configuration: either 16-bit or 32-bit filter size
- Mode configuration: either Id/Mask or Id/List mode



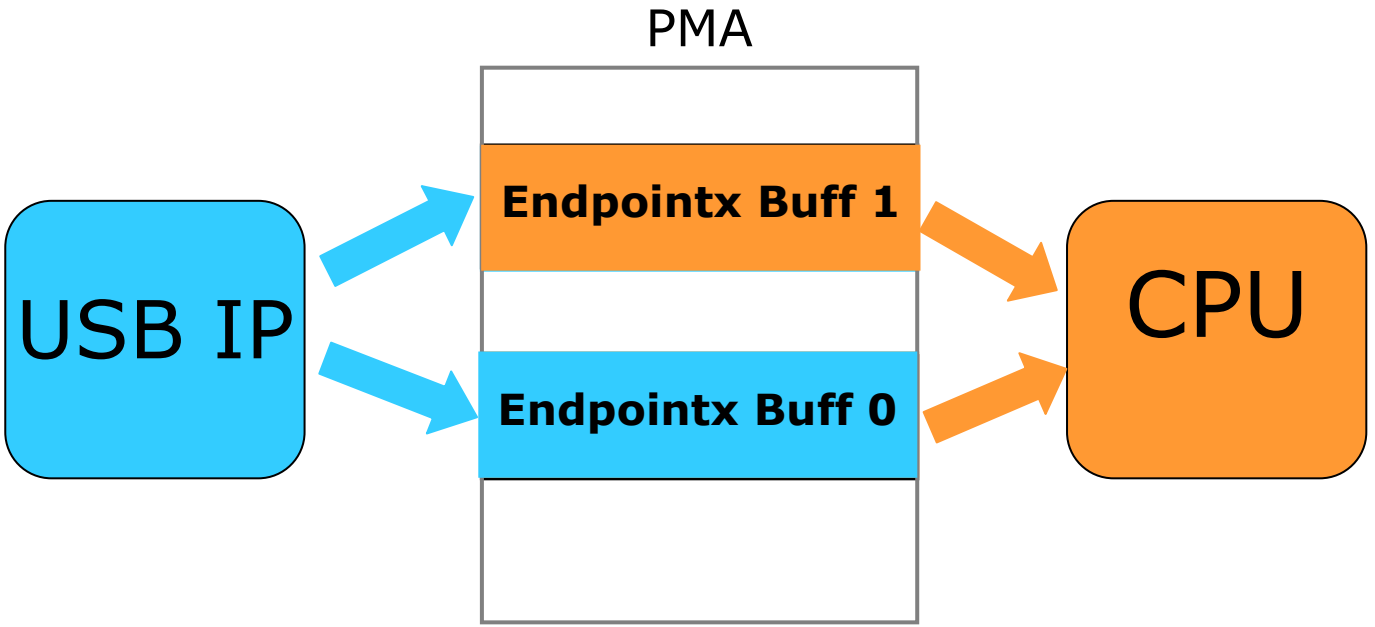
Universal Serial Bus Interface (USB Device)

USB Features

- Full speed USB 2.0 transfer.
- Configurable endpoints transfer mode type: control, bulk, interrupt and Isochronous.
- Configurable number of endpoints: up to 8 bidirectional endpoints and 16 mono-directional endpoints.
- USB suspend/resume support.
- Dedicated SRAM Area (**P**acket **M**emory **A**rea) up to 512bytes (shared with bxCAN).
- Dynamic buffer allocation according to the user needs.
- Special double buffer support for Isochronous and Bulk transfers.

Double Buffering transfer mode

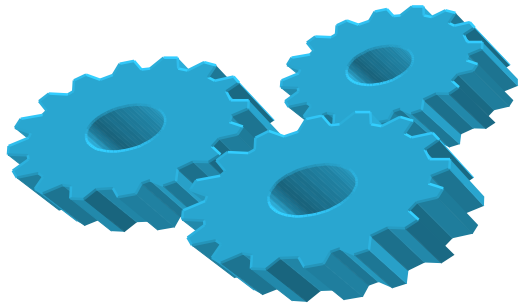
- Up to 7 mono-directional Double-buffered endpoints
- Highest possible transfer rate
- Number of NAKed transactions governed by the Application elaboration time.

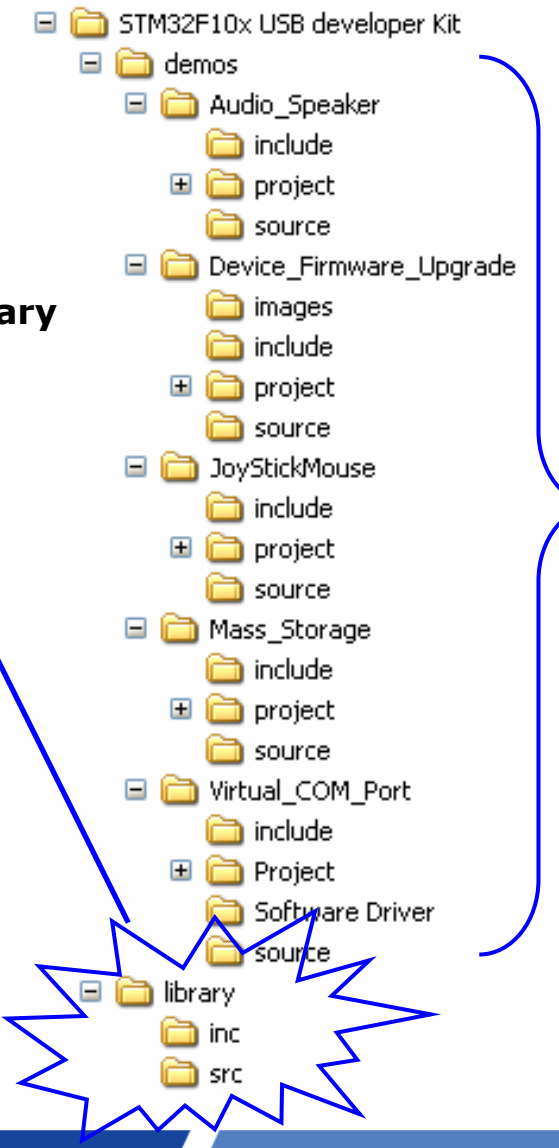


STM32F10x USB Developer's Kit

STM32 USB Library

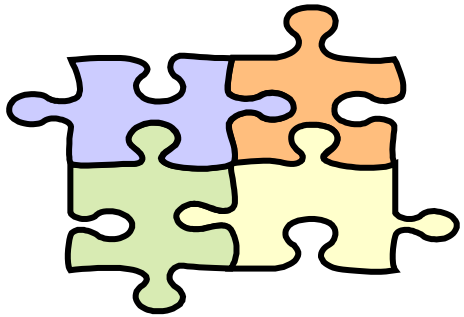
- **USB 2.0 full speed certified**
- **Strict ANSI-C**
- **Toolchain independent**
- **Independent from Firmware library**
- **Self documented**





STM32 USB Developer's Kit demos

- **Covers all USB transfer types**
- **Independent from any SW tool chain**
- **Running on STM32F10x-EVAL board**
- **Can easily be tailored to other target h/w**

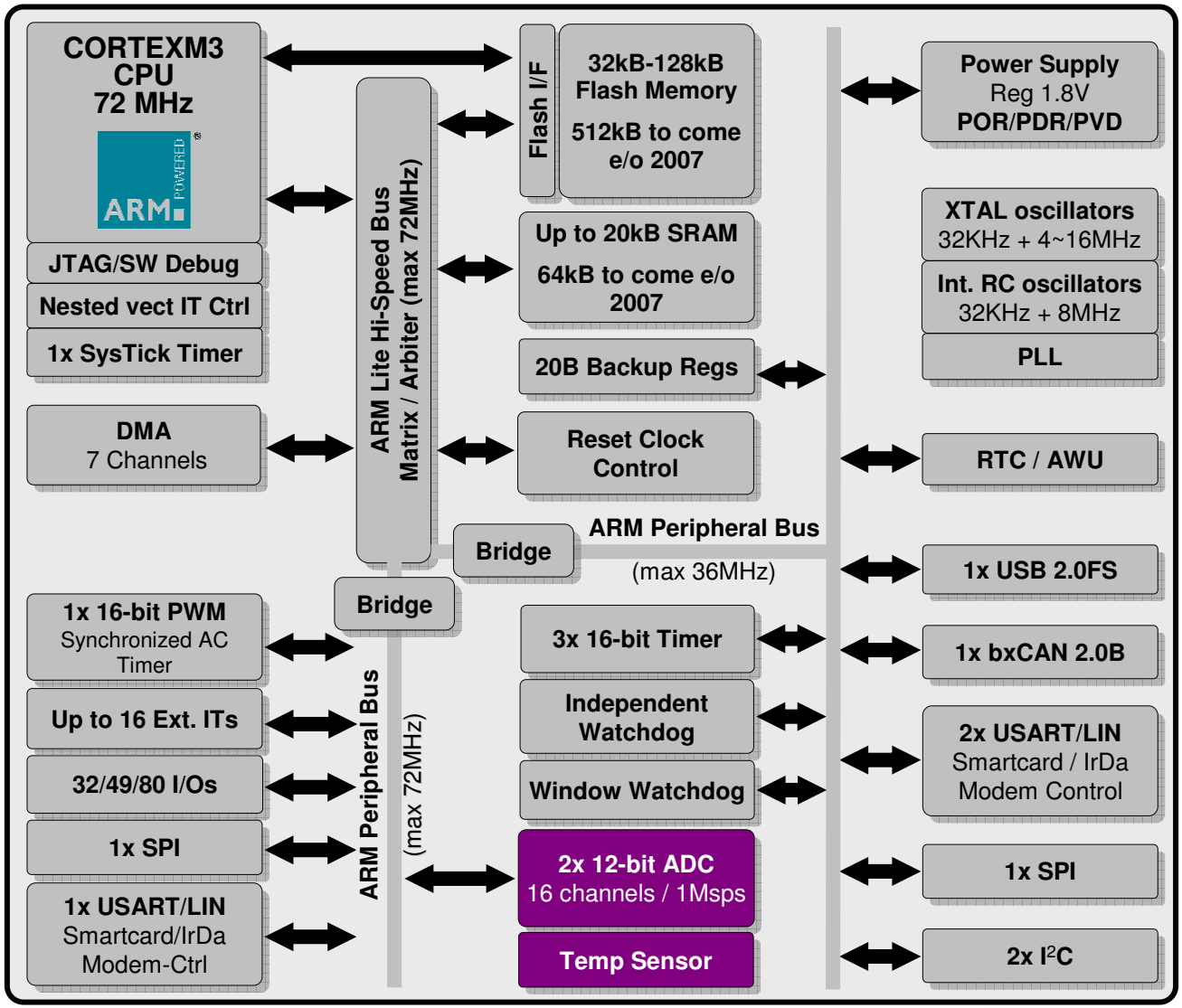


STM32
Device Firmware Upgrade (DFU) Demo

Analog-to-Digital Converter (ADC)

STM32F10x Series Block Diagram

- Up to 2x12-bits 1Msps ADC
- Up to 16 external channels
- Embedded temperature sensor, +/-1.5° linearity with T°



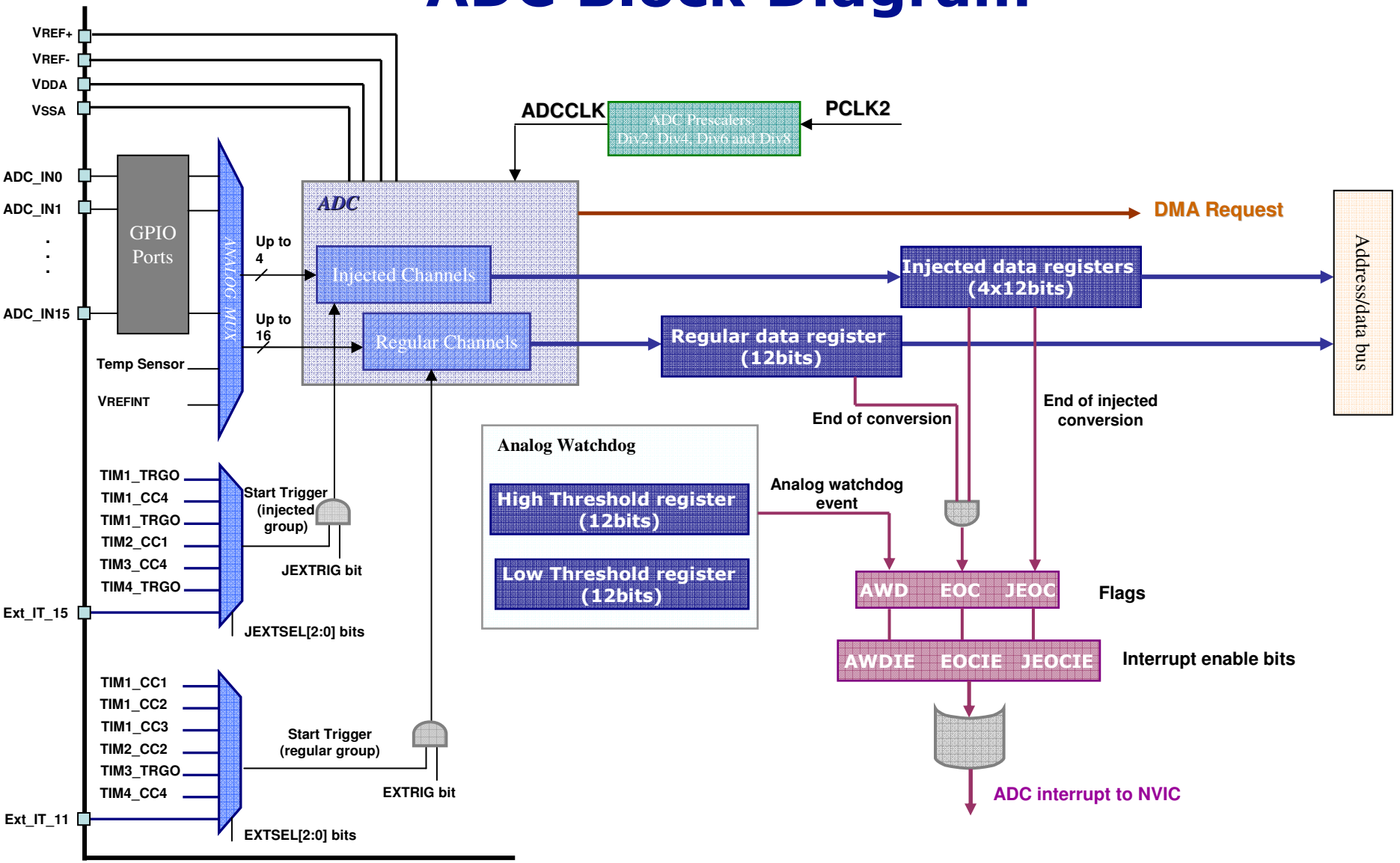
ADC Features (1/2)

- Single (Access Line) and Dual (Performance Line) ADC options
- Conversion rate 1MHz, 12-bit resolution
- ADC supply requirement: 2.4V to 3.6 V
- ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$ (V_{REF} pins only on 100pin pkg)
- Up to 18 multiplexed channels
  - 16 external channels
  - 2 internal channels: temperature sensor and voltage reference
- Grouped channels for conversion:
  - Regular group – up to 16 channels
  - Injected group – up to 4 channels
- Single, continuous and discontinuous conversion modes
- Dual modes (on devices with 2 ADCs): 8 variations

ADC Features (2/2)

- Sequencer-based Scan Mode for both Regular and Injected groups
- External trigger options for both Regular and Injected groups
- Channel-by-channel programmable sampling time
- Selectable Left/Right data alignment
- +/- Signed results from Injected groups
- Analog Watchdog with high and low thresholds
- Interrupt generation on:
  - End of Conversion (Regular groups)
  - End of Injected Conversion (Injected groups)
  - Analog Watchdog
- DMA capability
- Self-calibration

ADC Block Diagram



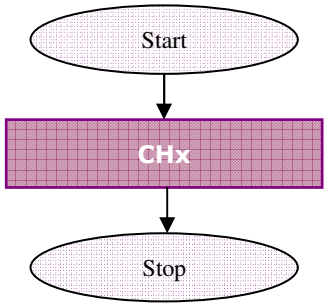
ADC Regular Conversion Group

- Programmable number of Regular channels: up to 16 channels
- Programmable sample time and channel order
- Conversion started by either:
  - Software through start bit
  - External trigger
    - Timer1 CC1
    - Timer1 CC2
    - Timer1 CC3
    - Timer2 CC2
    - Timer3 TRGO
    - Timer4 CC4
    - EXTI Line11
- Interrupt/DMA request at End of Conversion

ADC Injected Conversion Group

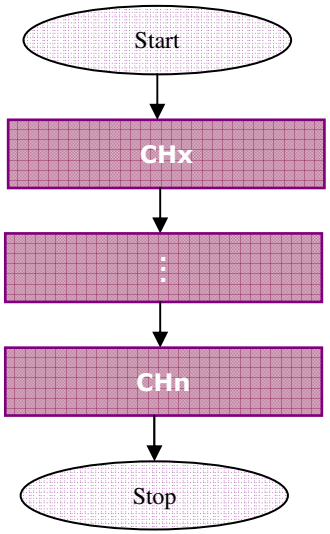
- Programmable number of Injected channels: up to 4 channels
- Programmable sample time and channel order
- Conversion started by either:
  - Software through start bit
  - JAUTO: automatic Injected group conversion after Regular group completes
  - External trigger
    - Timer1 TRGO
    - Timer1 CC4
    - Timer2 TRGO
    - Timer2 CC1
    - Timer3 CC4
    - Timer4 TRGO
    - EXTI Line15
- Programmable zero-offset for +/- signed conversions

ADC Conversion Modes: Single & Continuous

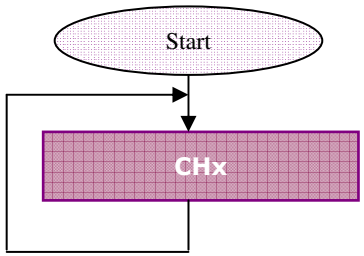


One channel

Single conversion mode

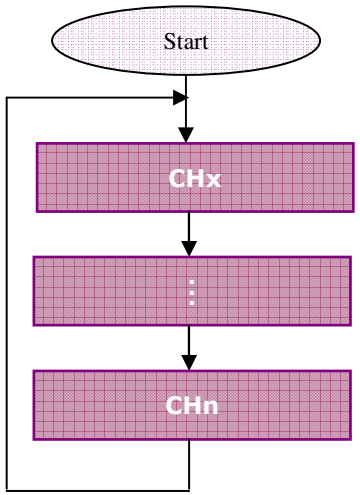


Multi-channels (Scan)
Single conversion mode



One channel

Continuous conversion mode



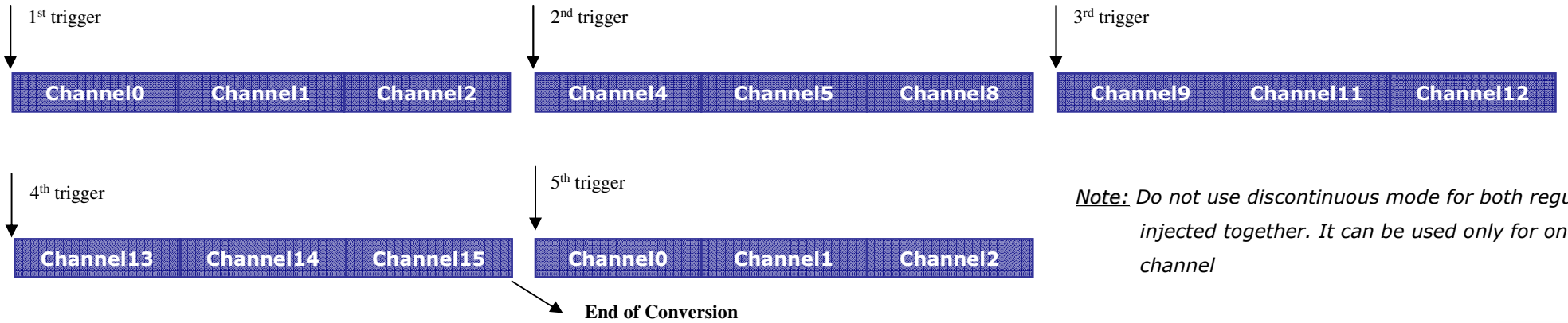
Multi-channels (Scan)
Continuous conversion mode

ADC Conversion Modes: Discontinuous

- Splits channel conversion sequence into sub-sequences
- Available for either Regular or Injected groups:
  - Up to 8 conversions per sub-sequence for Regular groups
  - Up to 3 conversions per sub-sequence for Injected groups

Example: - Conversion of channels: 0, 1, 2, 4, 5, 8, 9, 11, 12, 13, 14 and 15

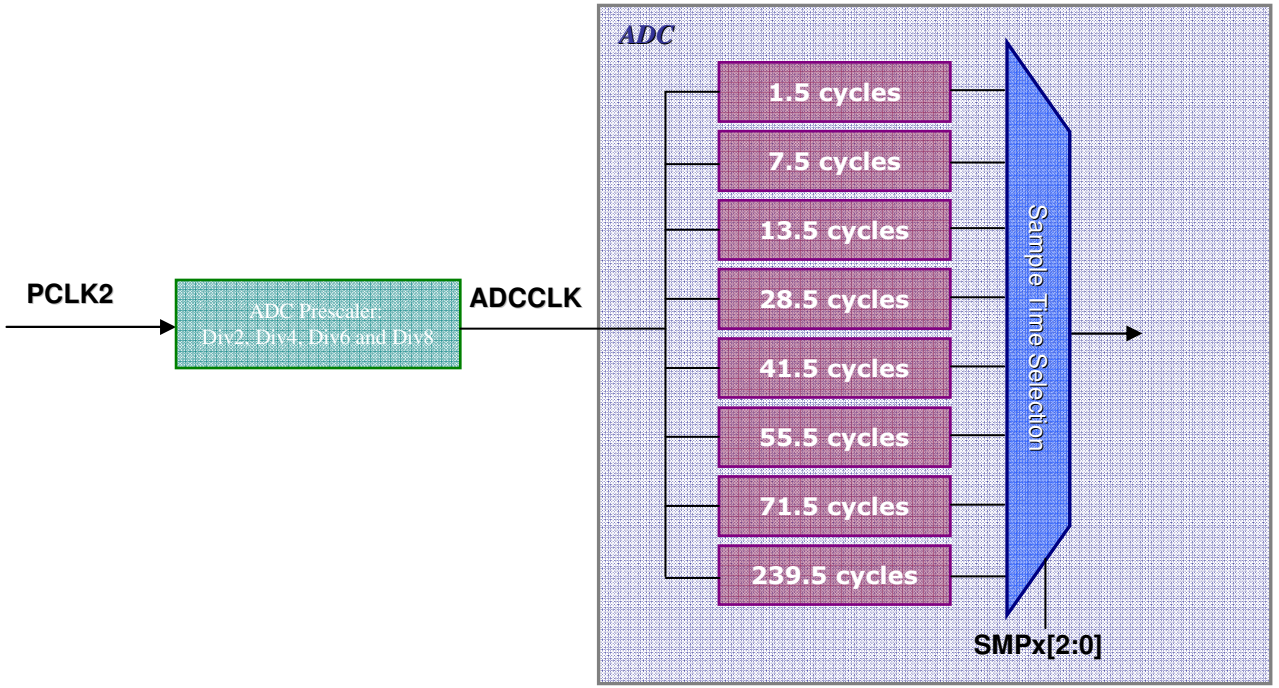
- Discontinuous mode Number of channel is 3



Note: Do not use discontinuous mode for both regular and injected together. It can be used only for one group channel

Analog Sample Time

- ADCCLK up to 14MHz derived from PCLK2 via prescaler (Div2,Div4,Div6,Div8)
- Programmable sample time for each channel:
  - 1.5 cycles
  - 7.5 cycles
  - 13.5 cycles
  - 28.5 cycles
  - 41.5 cycles
  - 55.5 cycles
  - 71.5 cycles
  - 239.5 cycles



- Total conversion = Sample time + 12.5 cycles
- At 14MHz, sample time of 1.5cycles, total conversion time = **1µs** (14 cycles)

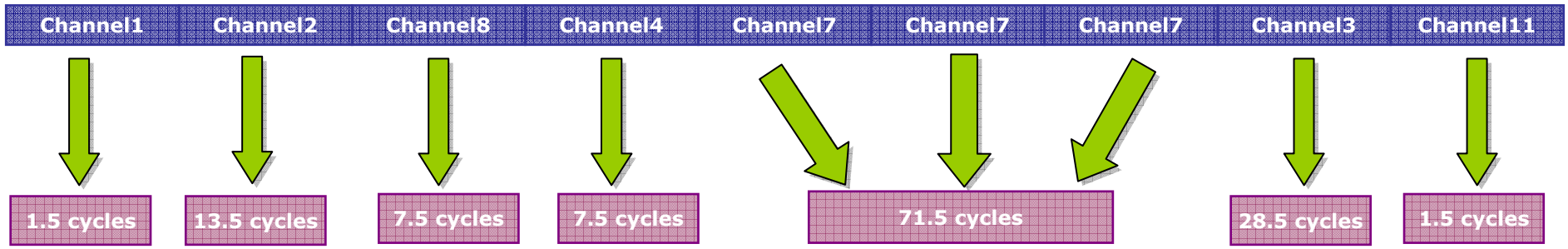
Sequencer

- Up to 16 conversions with different order, different sampling time and oversampling possibility.

Example: - Conversion of channels: 1, 2, 8, 4, 7, 3 and 11

- Different sampling time.

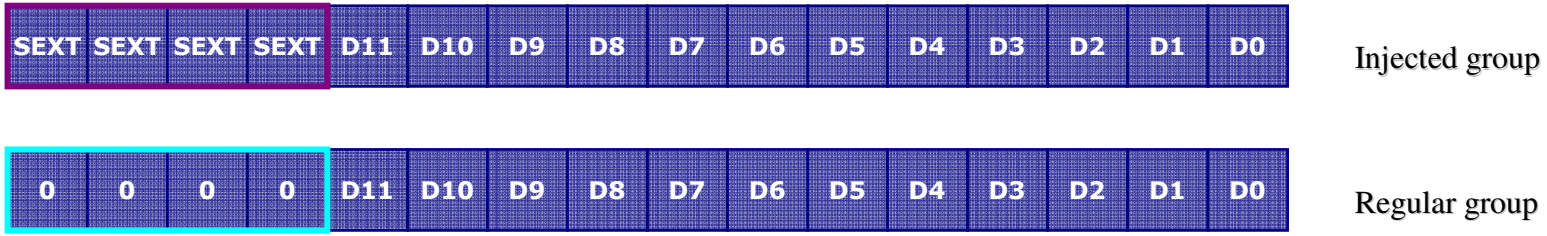
- Oversampling of channel 7.



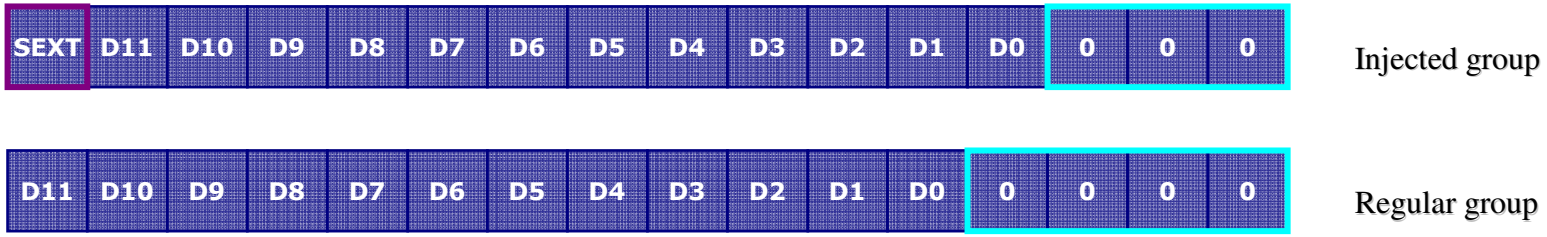
ADC Data Alignment

- One bit data align selection: right or left
- Sign extension for Injected group

Right alignment

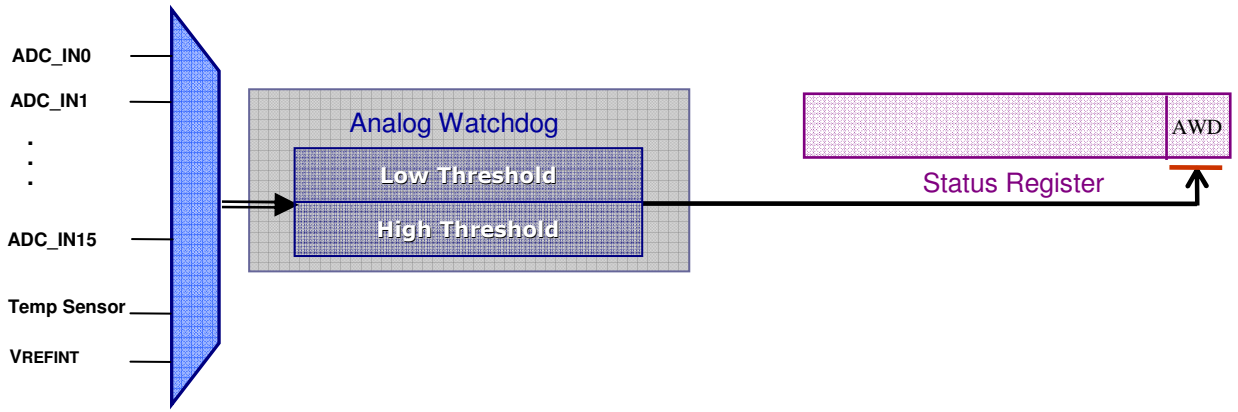


Left alignment



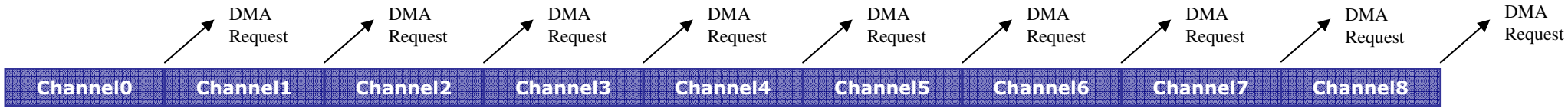
ADC Analog Watchdog

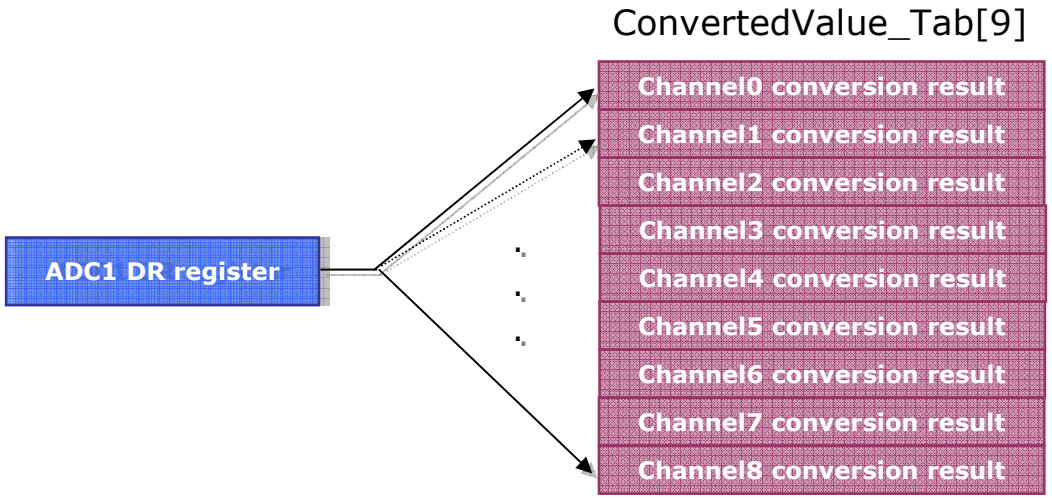
- 12-bit programmable analog watchdog with high and low thresholds
- Enabled on zero, one or all channels, regular and/or injected
- Interrupt generation on low or high threshold detection



DMA

- DMA request generated on each ADC1 end of regular channel conversion
- In dual modes, ADC2 and ADC1 results transferred in 32-bits of ADC1_DR

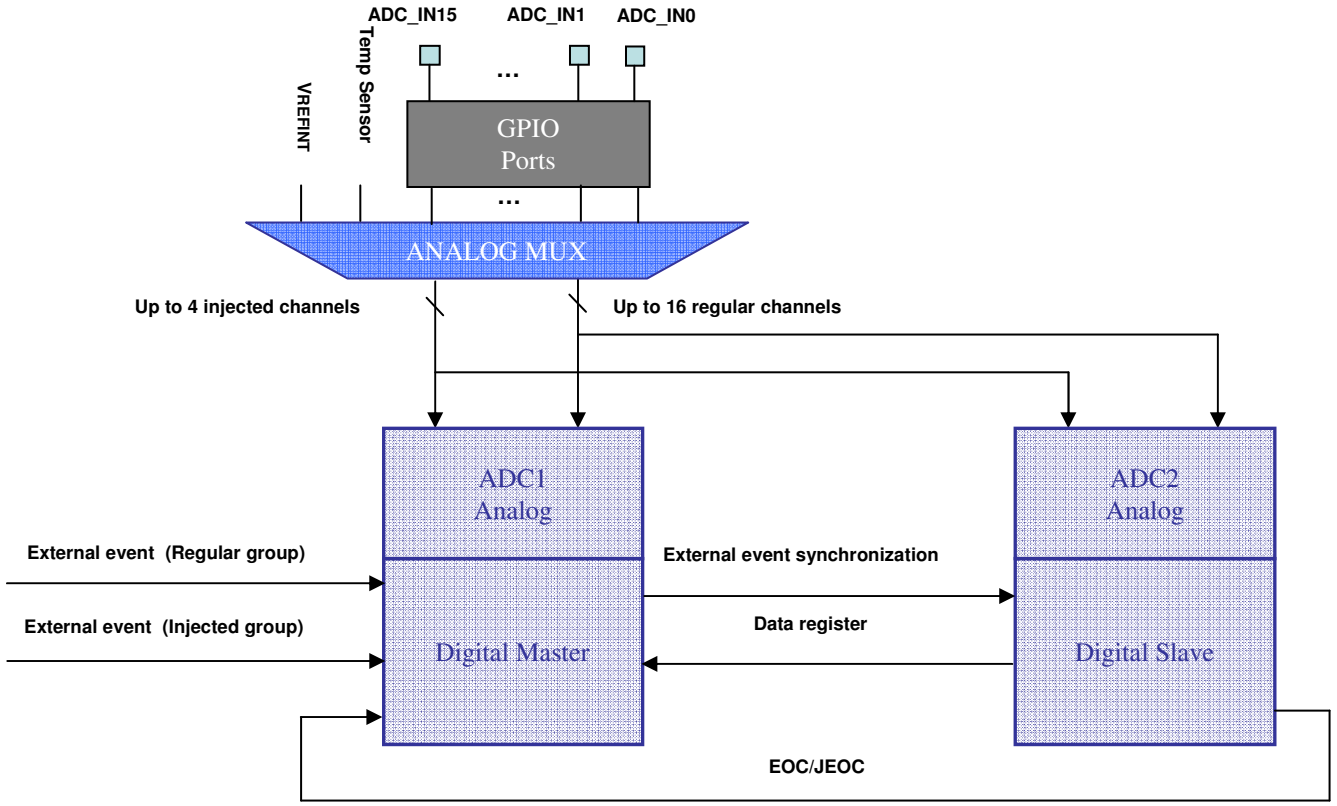




Example: - Conversion of Regular group
- DMA triggered by End of Conversion
- Results transferred to SRAM array by DMA
- DMA Destination address auto incremented
- EOC flag cleared by DMA access to ADCR1_DR

ADC Dual Modes (1/9)

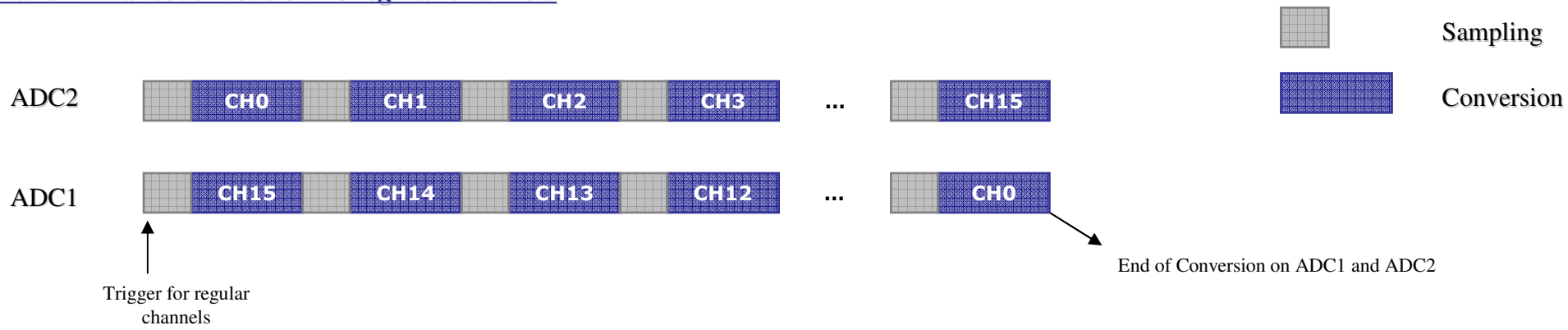
- Available in devices with two ADCs: ADC1 master and ADC2 slave
- Independent Dual Mode
- 8 Synchronised Dual Modes



ADC Dual Modes (2/9)
Regular Simultaneous Mode

- Converts Regular groups
- External trigger source routed via ADC1 (simultaneous trigger provided to ADC2)
- End of Conversion flag is generated when group conversions are complete
- Results for both ADCs stored in ADC1 Regular data register (32bits)
- Use DMA for efficient data transfer

Regular simultaneous mode on 16 regular channels

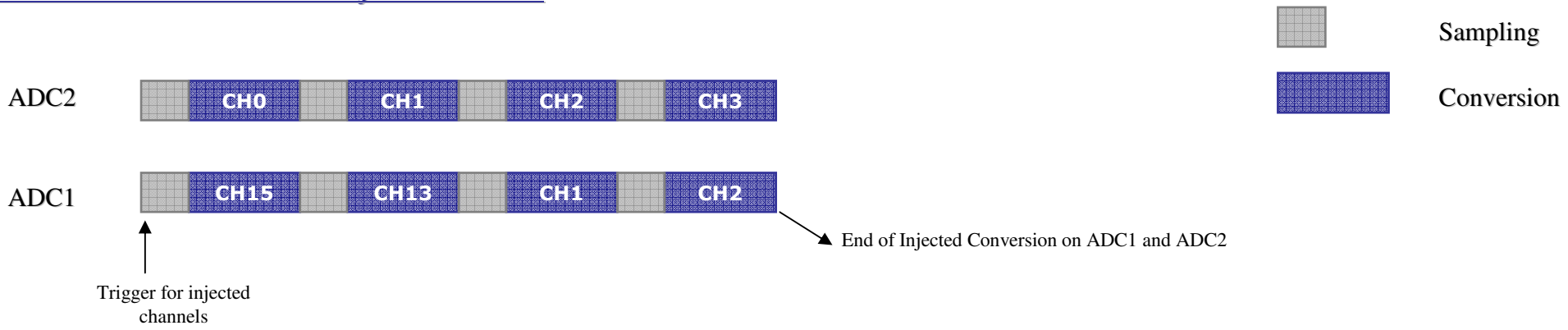


Note: Do not sample the same channel at the same time on each ADC

ADC Dual Modes (3/9)
Injected Simultaneous Mode

- Converts Injected groups
- External trigger source routed via ADC1 (simultaneous trigger provided to ADC2)
- End of Injected Conversion flags are generated when group conversions are complete
- Results stored in Injected data registers of each ADC

Injected simultaneous mode on 4 injected channels

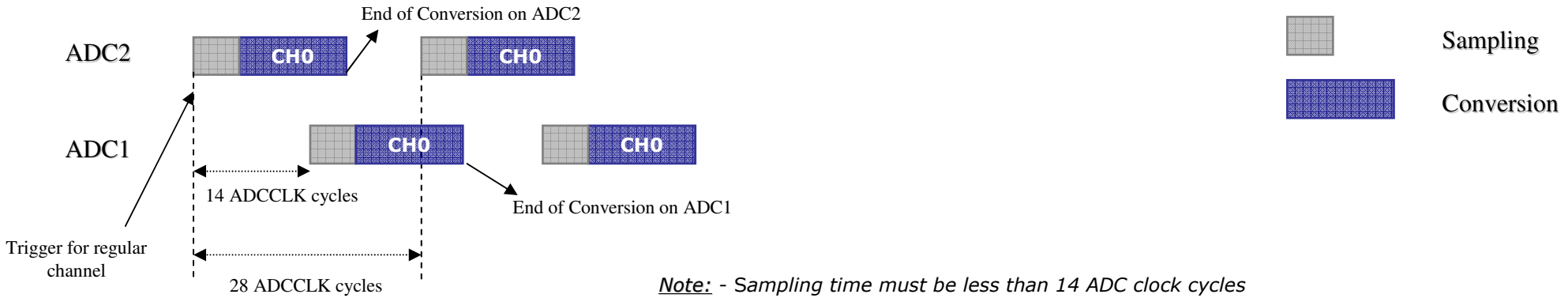


Note: Do not convert the same channel on the two ADCs

ADC Dual Modes (4/9)
Slow Interleaved Mode

- Converts Regular groups (only one channel)
- External trigger source routed via ADC1
  - Trigger routed to start ADC2 conversion immediately
  - ADC1 conversion begins after 14cycle delay
- End of Conversion flag is generated after each conversion is complete
- Results for both ADCs stored in ADC1 Regular data register (32bits)
- Next conversion on each ADC automatically started after 28 cycles
- Use DMA for efficient data transfer

Slow Interleaved mode on 1 regular channel

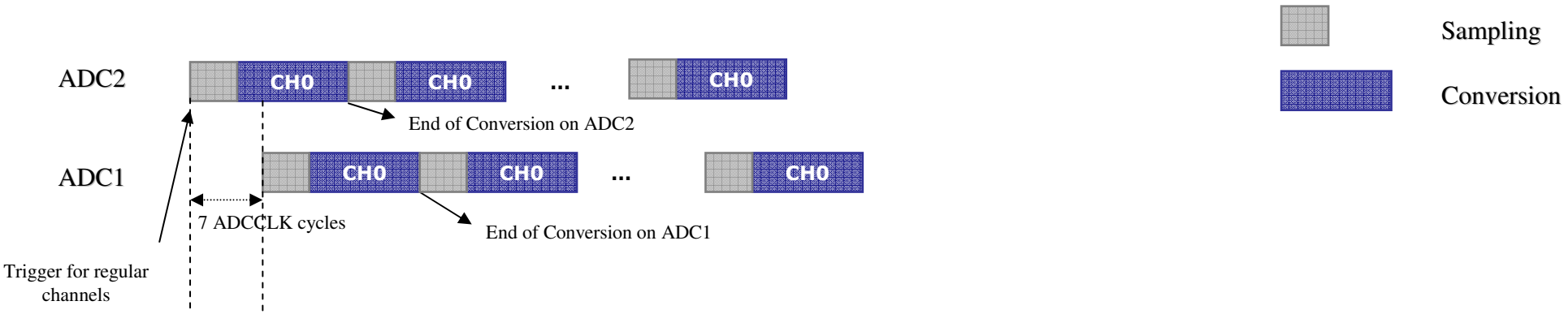


Note: - *Sampling time must be less than 14 ADC clock cycles*

ADC Dual Modes (5/9)
Fast Interleaved Mode

- Converts Regular groups (usually one channel)
- External trigger source routed via ADC1
  - Trigger routed to start ADC2 conversion immediately
  - ADC1 conversion begins after 7cycle delay
- End of Conversion flag is generated when each conversion is complete
- Results for both ADCs stored in ADC1 Regular data register (32bits)
- Use DMA for fast & efficient data transfer

Fast Interleaved mode on 1 regular channel in continuous conversion mode

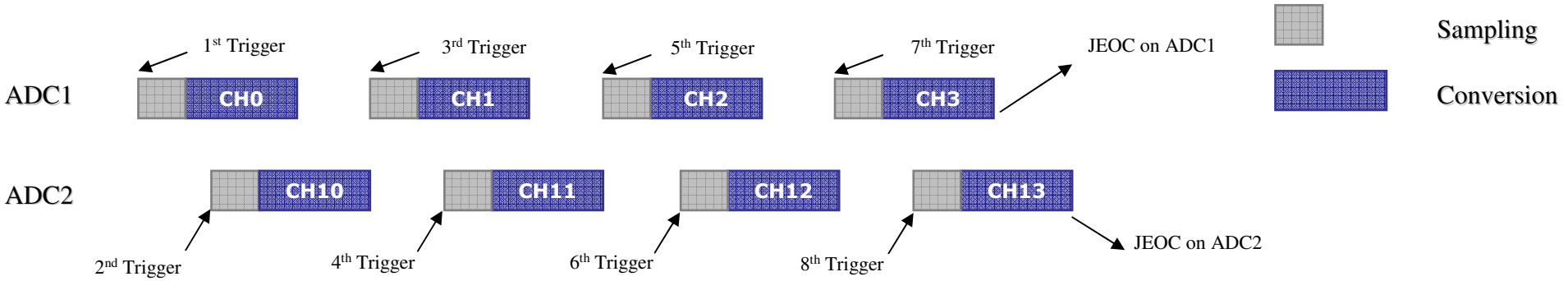


Note: - *Sampling time must be less than 7 ADC clock cycles*

ADC Dual Modes (6/9)
Alternate Trigger Mode

- Converts Injected groups
- External trigger source routed via ADC1
  - ADC1 and ADC2 conversions triggered alternately
  - Scan or Discontinuous Modes
- End of Conversion flags are generated when group conversions are complete
- Results stored in Injected data registers of each ADC

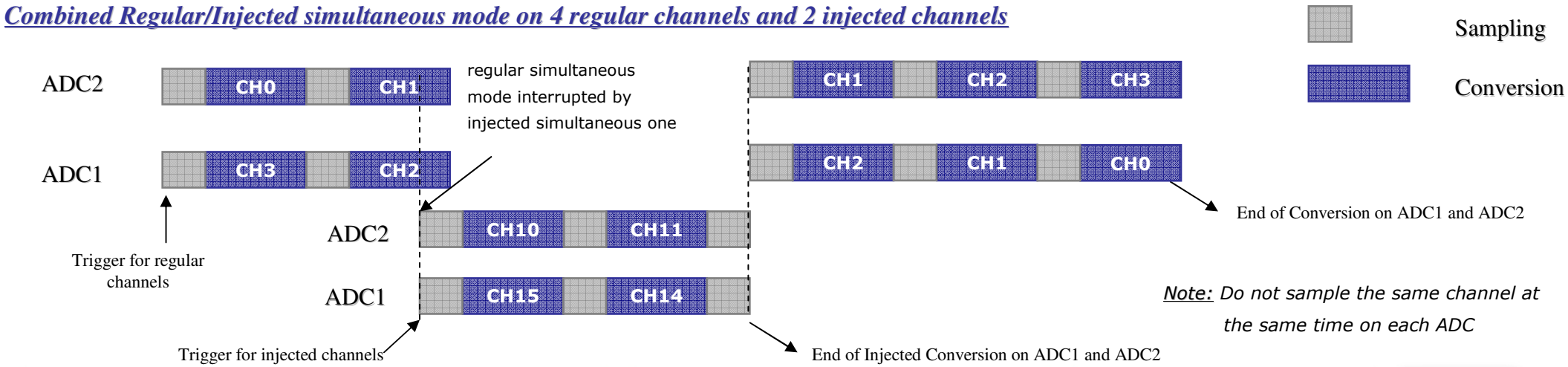
Alternate Trigger mode on 4 injected channels (injected discontinuous mode enabled)



ADC Dual Modes (7/9)

Combined Regular/Injected Simultaneous Mode

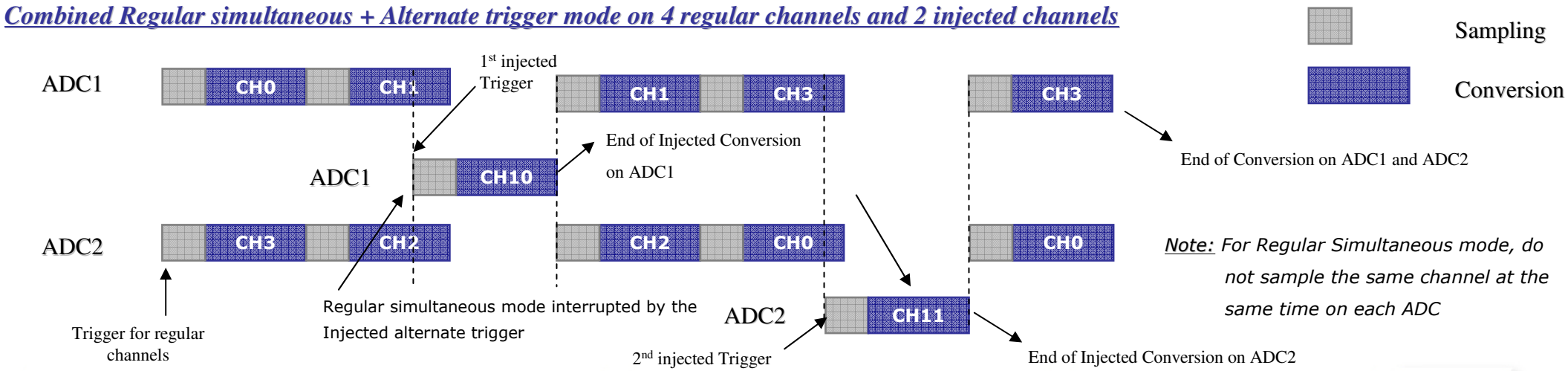
- Converts Regular and Injected groups
- External trigger source routed via ADC1
  - Simultaneous trigger fed to ADC2
  - Trigger for Injected conversions interrupts running Regular conversion
- End of Injected Conversion flags generated when Injected group conversions are complete
- End of Conversion flags are generated when Regular group conversions are complete
- Injected group results stored in Injected data registers of each ADC
- Regular group results stored in Regular data register of ADC1 (32 bits)



ADC Dual Modes (8/9)

Combined Regular Simultaneous & Alternate Trigger Mode

- Converts Regular and Injected groups
- External trigger source routed via ADC1
  - Simultaneous trigger fed to ADC2
  - Trigger for alternate Injected conversions interrupts running Regular conversion
- End of Injected Conversion flags generated when Injected group conversions are complete
- End of Conversion flags are generated when Regular group conversions are complete
- Injected group results stored in Injected data registers of each ADC
- Regular group results stored in Regular data register of ADC1 (32 bits)

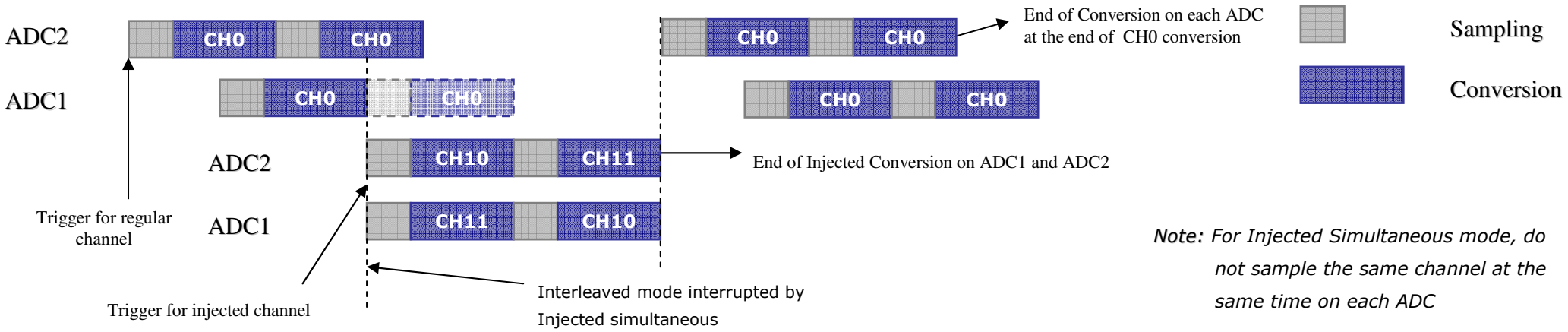


ADC Dual Modes (9/9)

Combined Fast Interleaved & Injected Simultaneous Mode

- Converts Regular and Injected groups
- External trigger source routed via ADC1
  - Trigger routed to start ADC2 conversion immediately, ADC1 conversion begins after 7cycle delay
  - Trigger for simultaneous Injected conversions interrupts running Regular conversion
- End of Injected Conversion flags generated when Injected group conversions are complete
- End of Conversion flags are generated when Regular group conversions are complete
- Injected group results stored in Injected data registers of each ADC
- Regular group results stored in Regular data register of ADC1 (32 bits)

Combined Injected simultaneous + Interleaved mode on 1 regular (continuous conversion) channel and 2 injected channels

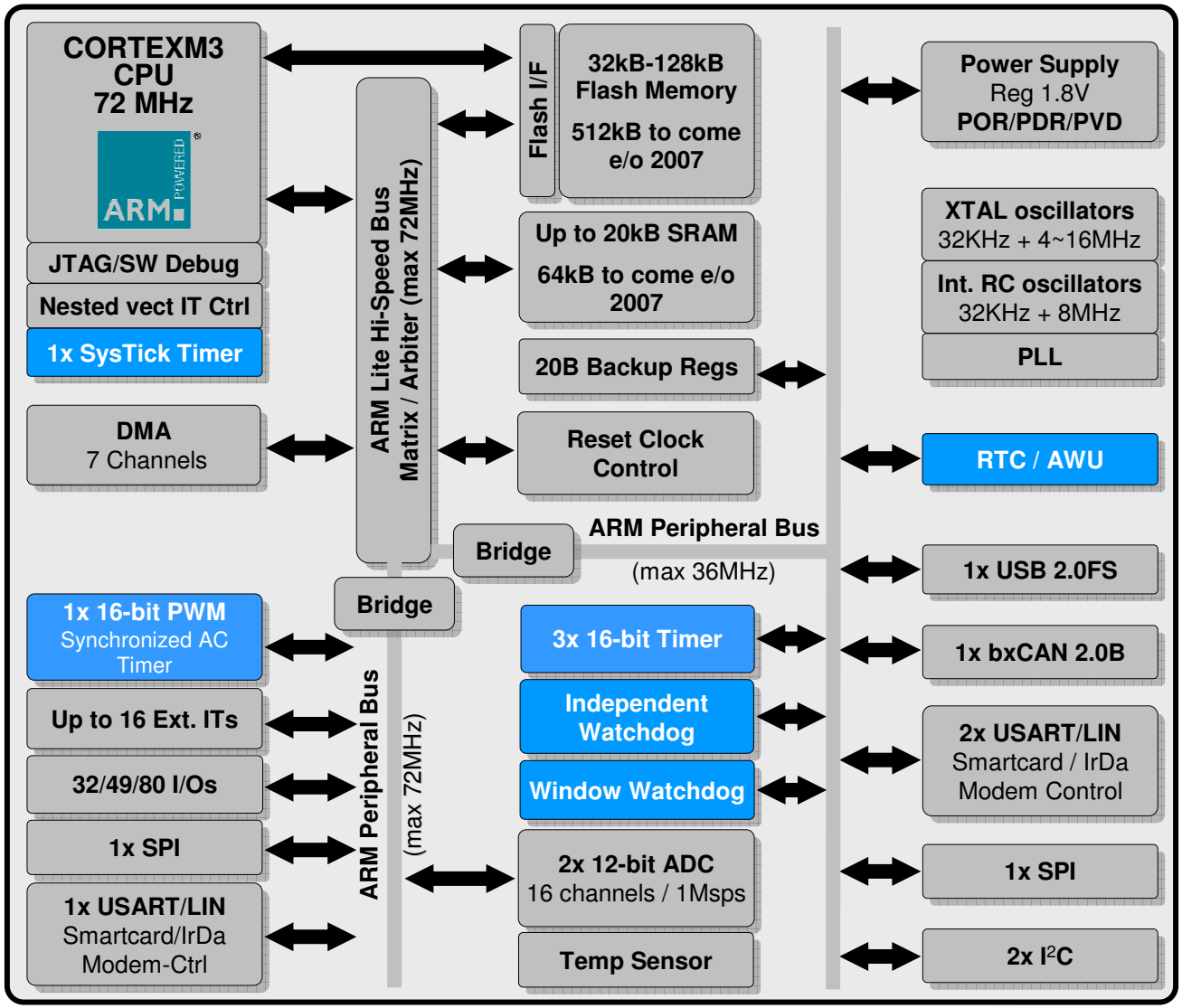


Note: For Injected Simultaneous mode, do not sample the same channel at the same time on each ADC

STM32 Timers

STM32F10x Series Block Diagram

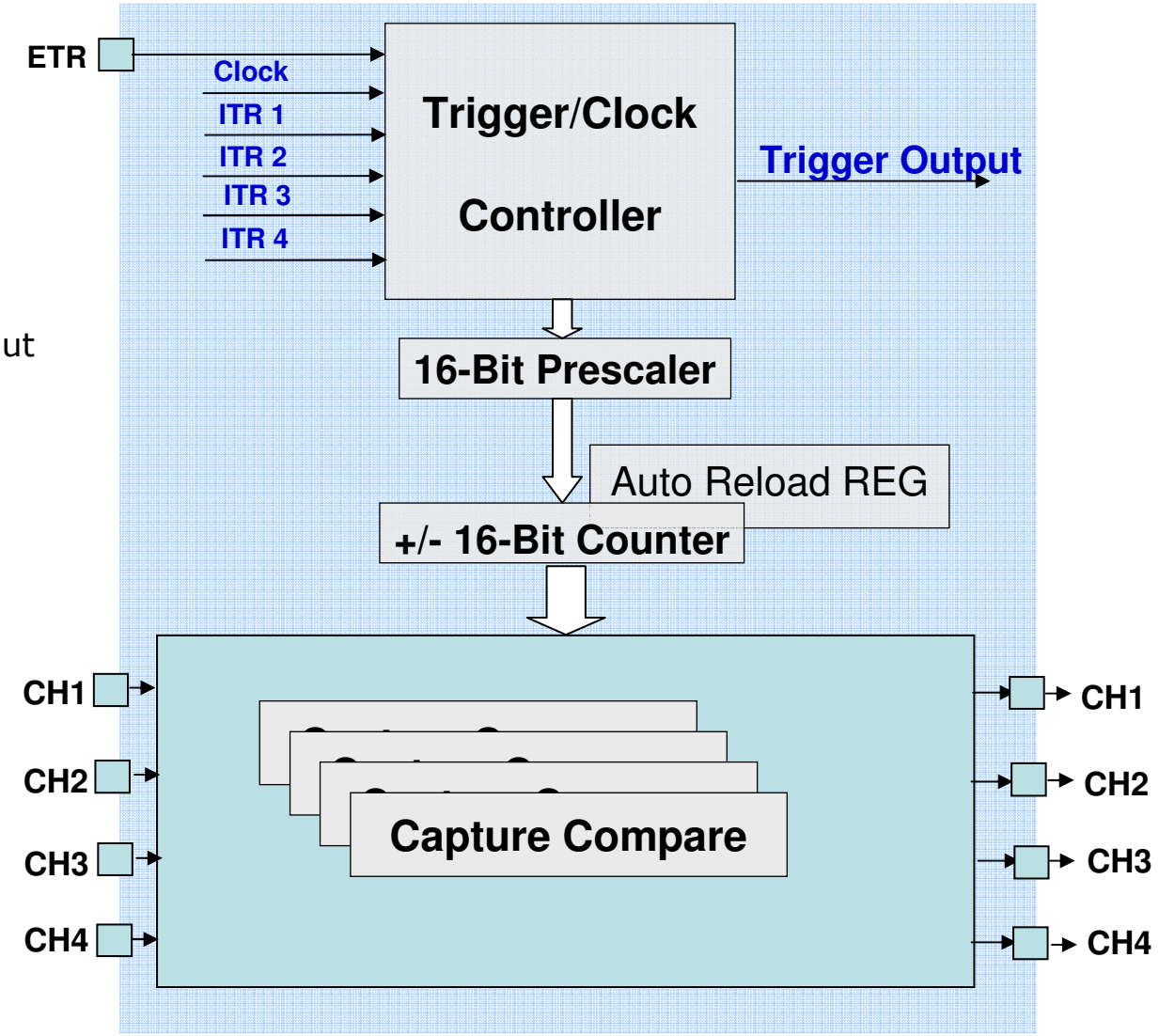
- 4 Timers w/ advanced control features
- Embedded low power RTC with V_{BAT} capability
- Dual Watchdog Architecture
- Cortex-M3 SysTick Timer



General Purpose & Advanced Control Timers

General Purpose Timer Overview

- TIM2, 3, 4 on Low Speed APB (APB1)
- Internal clock up to 72 MHz
- 16-bit Counter
  - Up, down and centred counting modes
  - Auto Reload
- 4 x 16-bit Capture/Compare Channels
  - Programmable channel direction: input/output
  - Input Capture, PWM Input Capture Modes
  - Output Compare, PWM, One Pulse Modes
- Synchronization
  - Timer Master/Slave
  - Synchronisation with external trigger
  - Triggered or gated modes
  - Serial and Parallel Multi-timer Cascade
- Encoder interface
- Hall sensor interface
- Independent IRQ/DMA Requests:
  - At each Update Event
  - At each Capture Compare Events
  - At each Input Trigger
- Debug mode

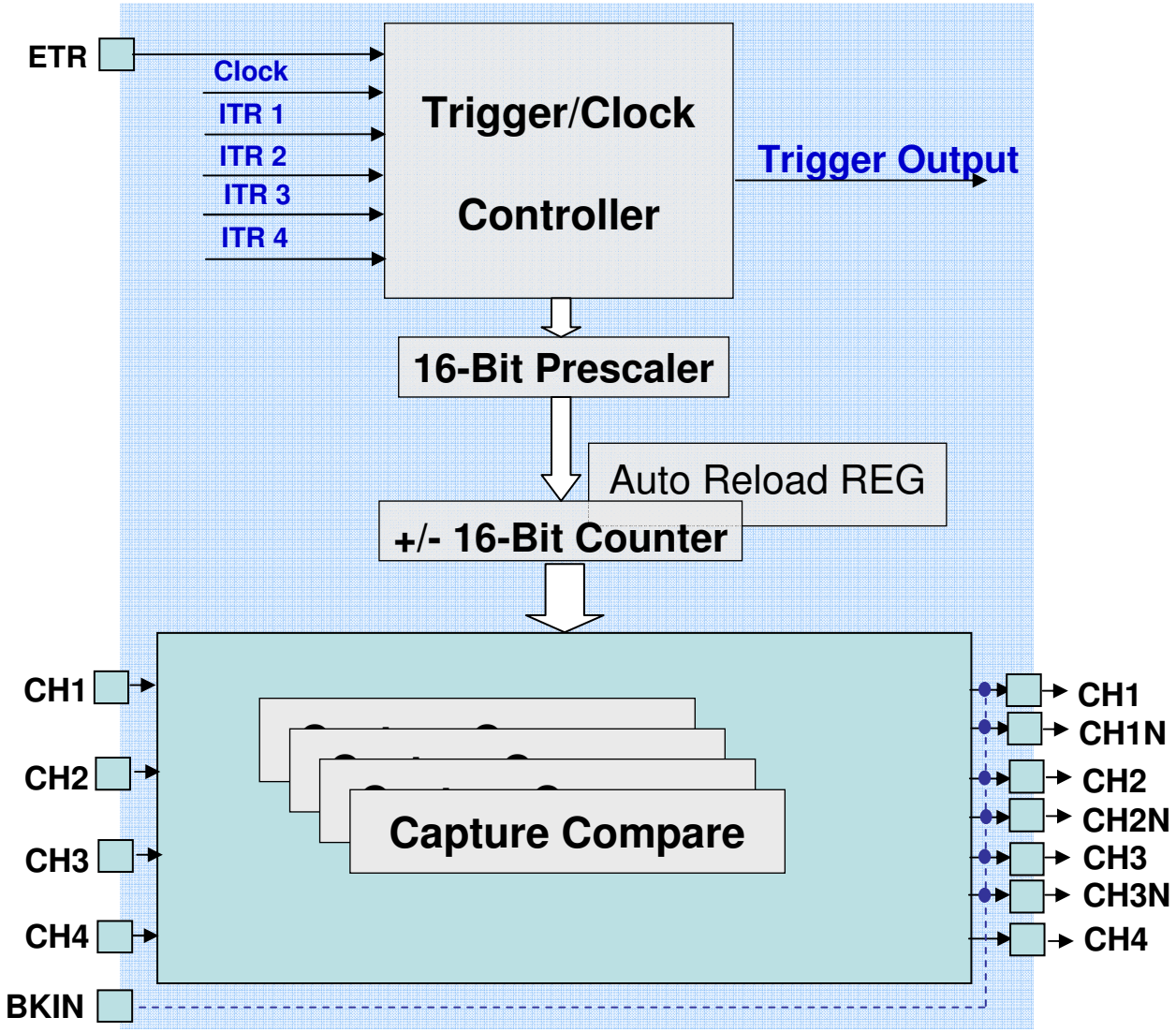


Advanced Timer Overview

- TIM1 on High Speed APB (APB2)
- Internal clock up to 72 MHz
- As GP Timers, plus…

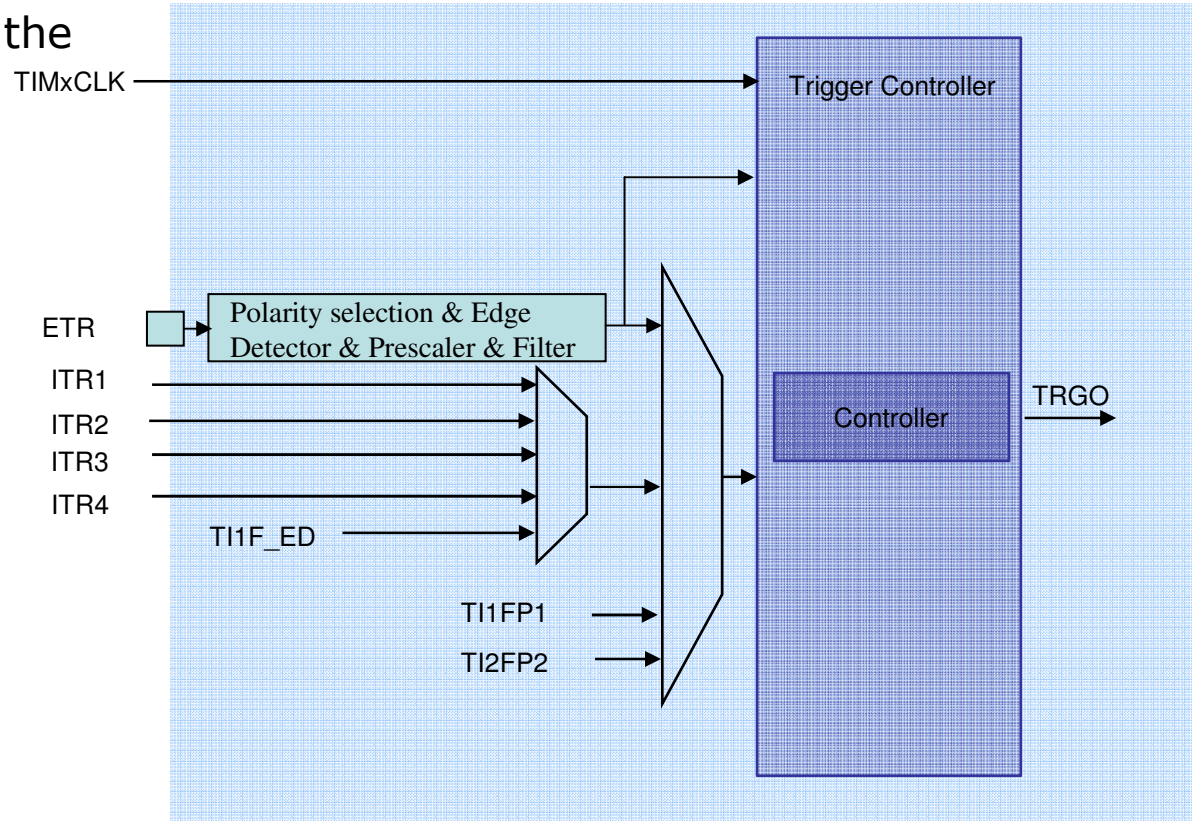
- Complementary outputs
- Repetition counter
- Channel programmable polarity
- Channel programmable idle state
- Preload bits (e.g. 6-step PWM generation)
- Break Event
  - Break Input (BKIN)
  - Clock Security System

- Configurable lockable levels

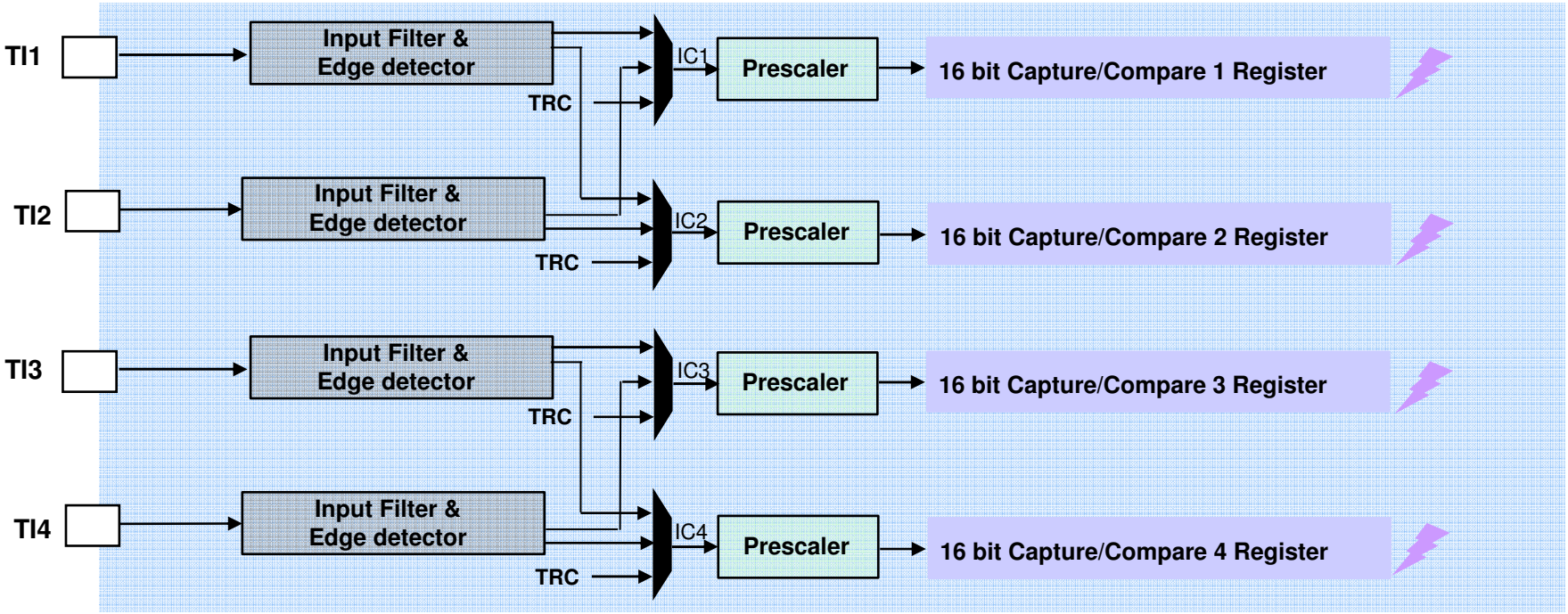


Counter Clock Selection

- Clock can be selected from 8 sources
  - Internal clock TIMxCLK provided by the RCC
  - Internal trigger input 1 to 4:
    - ITR1 / ITR2 / ITR3 / ITR4
    - Using another timer as a prescaler
  - External Capture Compare pins
    - Pin 1: TI1FP1 or TI1F_ED
    - Pin 2: TI2FP2
  - External pin ETR
    - Enable/Disable bit
    - Programable polarity
    - 4 Bits External Trigger Filter
    - External Trigger Prescaler:
      - Prescaler off
      - Division by 2
      - Division by 4
      - Division by 8



Input Capture Mode

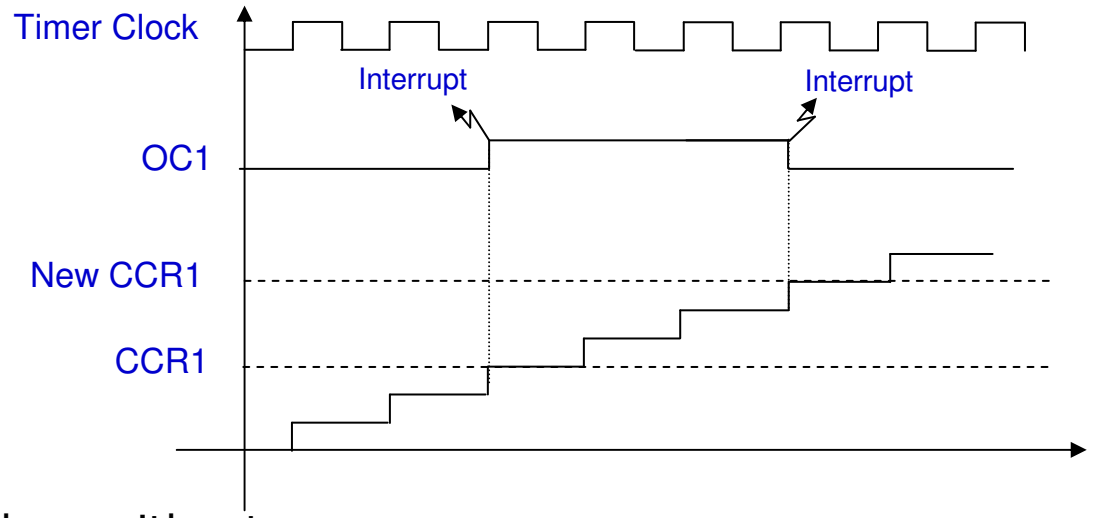


- IC1, IC2, IC3 and IC4 are specific as they can be independently mapped by software on TI1, TI2, TI3 or TI4.
- 4x16-bit capture compare registers are programmable to be used to latch the value of the counter after a transition detected by the corresponding Input Capture.
- When a capture occurs, the corresponding CCXIF flag is set and an interrupt or a DMA request can be sent if they are enabled.
- “Overcapture” flag set if second capture occurs before previous capture is cleared

Output Compare Mode

The Output Compare is used to control an output waveform or indicate when a period of time has elapsed.

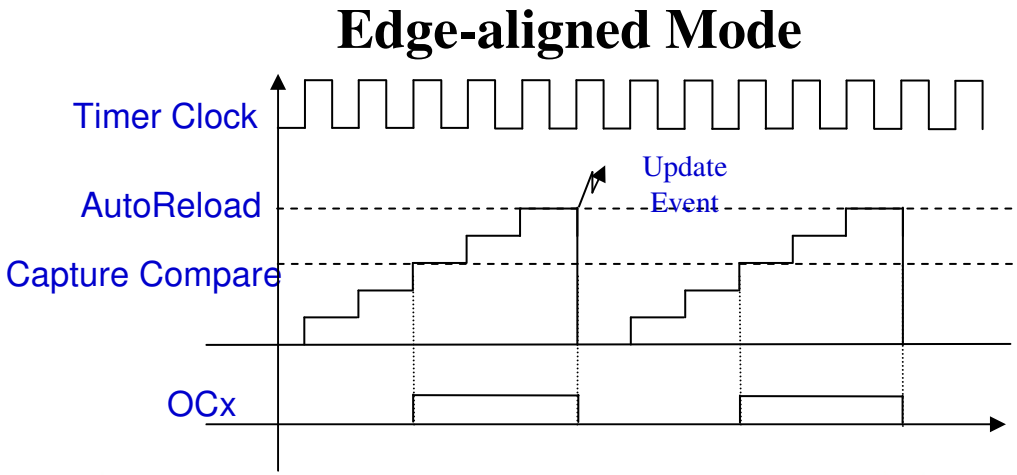
- When a match is found between the capture/compare register and the counter:
  - The corresponding output pin is assigned to the programmable Mode, it can be:
    - Set
    - Reset
    - Toggle
    - Remain unchanged
  - Set a flag in the interrupt status register
  - Generates an interrupt if the corresponding interrupt mask is set
  - Send a DMA request if the corresponding enable bit is set

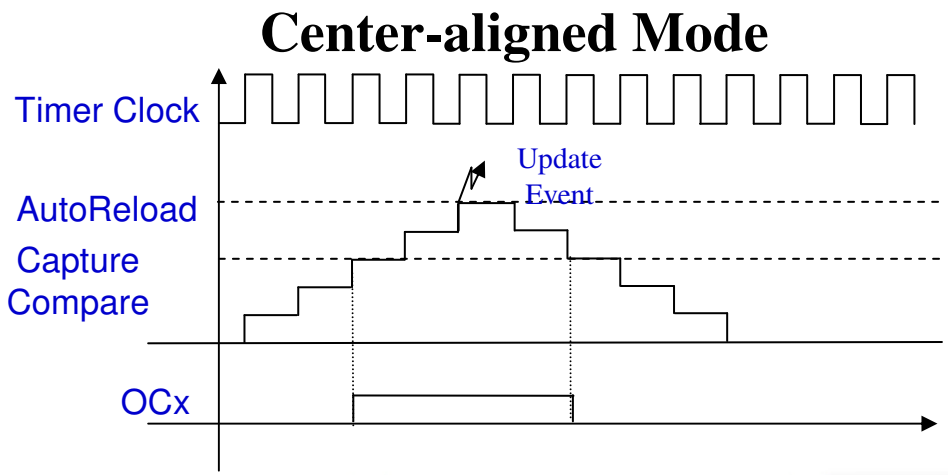


- The CCRx registers can be programmed with or without preload registers

PWM Mode

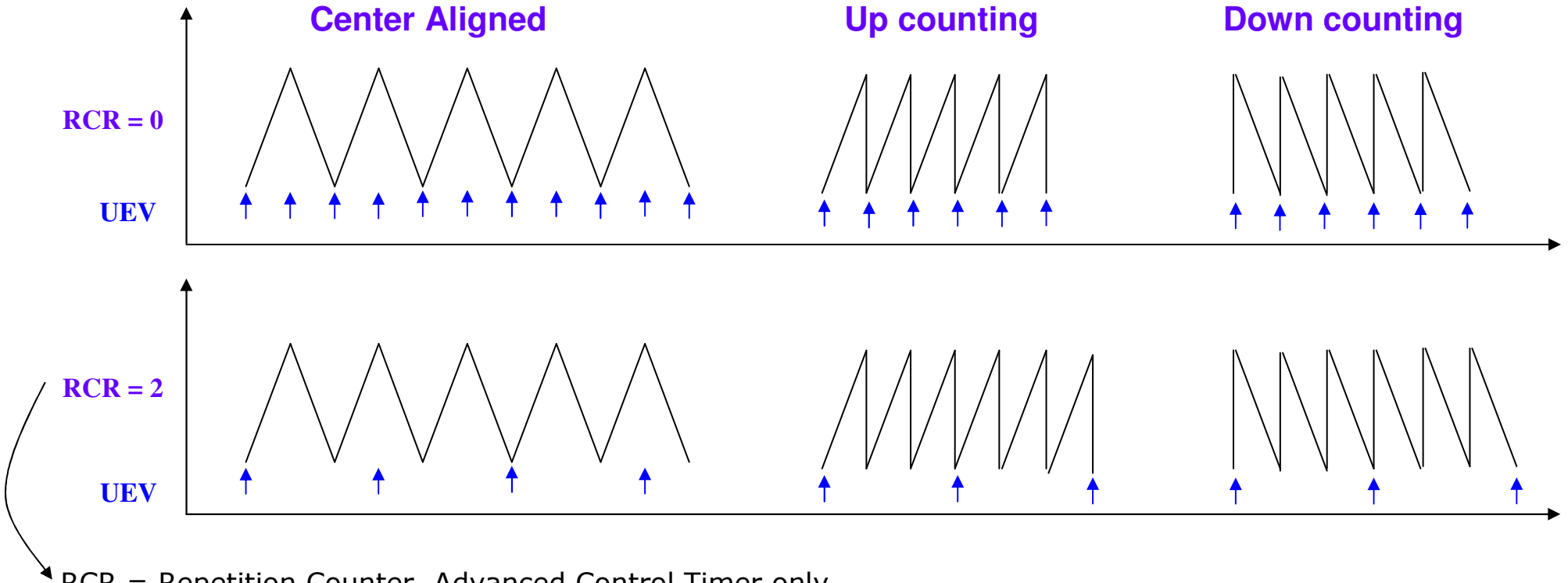
- The PWM mode allows to generate:
  - 4 independent signals for TIM1, plus 3 complementary signals with individually programmable dead time insertion.
  - 4 independent signals for TIM2, 3 and 4
  - The frequency and a duty cycle determined as follow:
    - One auto-reload register to defined the PWM period.
    - Each PWM channel has a Capture Compare register to define the duty cycle.
  - ➔ Example: to generate a 40 KHz PWM signal w/ duty cycle of 50% on TIM1 clock at 72MHz:
    - Load Prescaler register with 0 (counter clocked by TIM1CLK/(0+1)), Auto Reload register with 1799 and CCRx register with 899
- There are two configurable PWM modes:
  - Edge-aligned Mode
  - Center-aligned Mode





Counter Modes

- Three Counter Modes
  - Up Counting
  - Down Counting
  - Centre-Aligned Mode

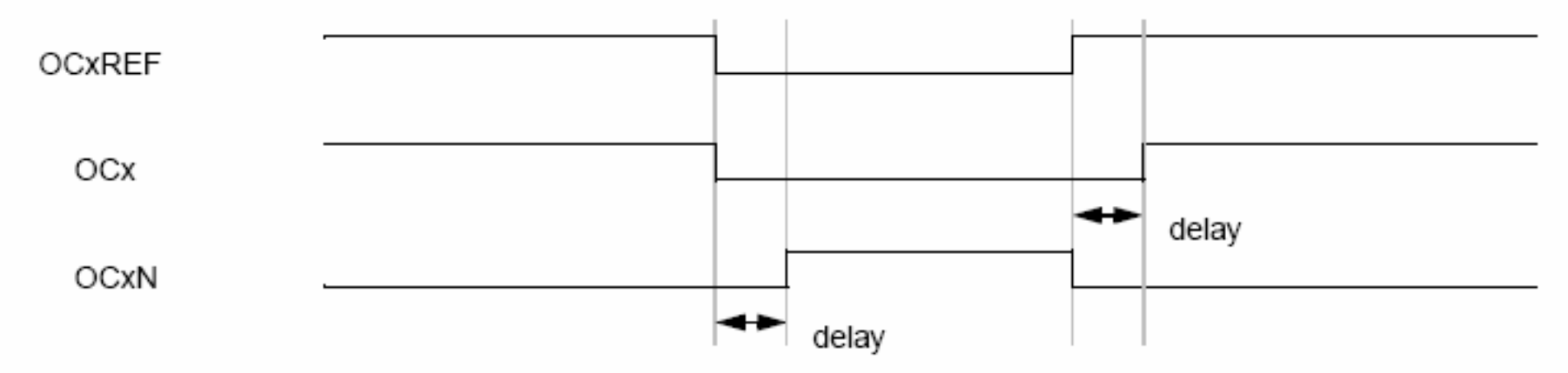


RCR = Repetition Counter, Advanced Control Timer only

Advanced Control timer TIM1
Complementary PWM outputs for motor control

- This mode allows the TIM1 to:
  - Output two complementary signals for each three channels.
  - Output two independent signals for each three channels.
  - Manage the dead-time between the switching-off and the switching-on instants of the outputs.
- One reference waveform OCx_{REF} to generate 2 outputs OCx and OCxN for the three channels.
- Full modulation capability (0 and 100% duty cycle), edge or center-aligned patterns
- Dedicated interrupt and DMA requests for TIM1 period and duty cycles updating.
- Three programmable write protection levels
  - Level1: Dead Time and Emergency enable are locked.
  - Level2: Level1 + Polarities and Off-state selection for run and Idle state are locked.
  - Level3: Level2 + Output Compare Control and Preload are locked.

Advanced Control timer TIM1
Dead Time Insertion & Timer Write Protection



- Dead Time Insertion
  - Rising edges of both OC and OC_N delayed by programmable dead time
- Timer Write Protection
  - Level1: Dead Time and Emergency enable are locked.
  - Level2: Level1 + Polarities and Off-state selection for run and Idle state are locked.
  - Level3: Level2 + Output Compare Control and Preload are locked.

Advanced Control timer TIM1
The break function

- The break can be generated by:
  - The BRK input which has a programmable polarity and an enable bit BKE
  - The Clock Security System
- When a break occurs:
  - The MOE bit: Main Output Enable is cleared
  - Each output channel is driven with the level programmed in the OISx bit
  - The break status flag is set.
  - An interrupt or a DMA request can be generated if the BIE bit is set or if the BDE bit is set.
- Break applications:
  - If the AOE: Automatic Output Enable bit is set, the MOE bit is automatically set again at the next update event UEV

    ⇒ This can be used to perform a regulation.
  - If the AOE is Reset, the MOE remains low until you write it to '1' again

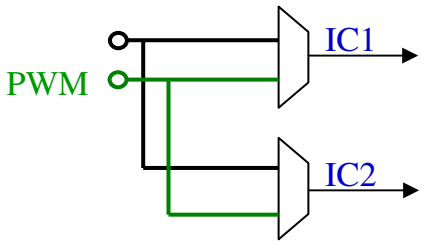
    ⇒ In this case, it can be used for security and you can connect the break input to an alarm from power drivers, thermal sensors or any security components.

PWM Input Mode

PWMI Configuration tips:

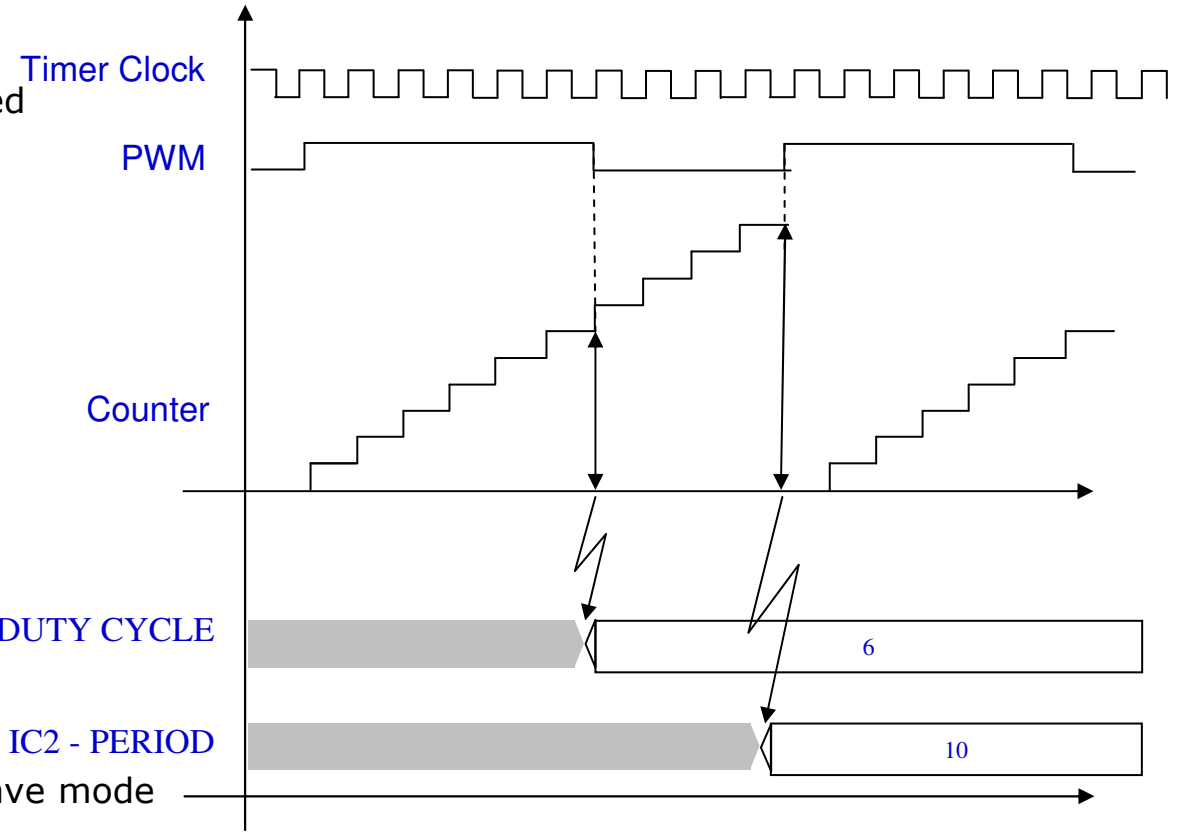
- IC1 and IC2 must be configured to be connected together to the PWM signal:

⇨ IC1 and IC2 are redirected internally to be mapped to the same external pin TI1 or TI2.



- IC1 and IC2 active edges must have opposite polarity.

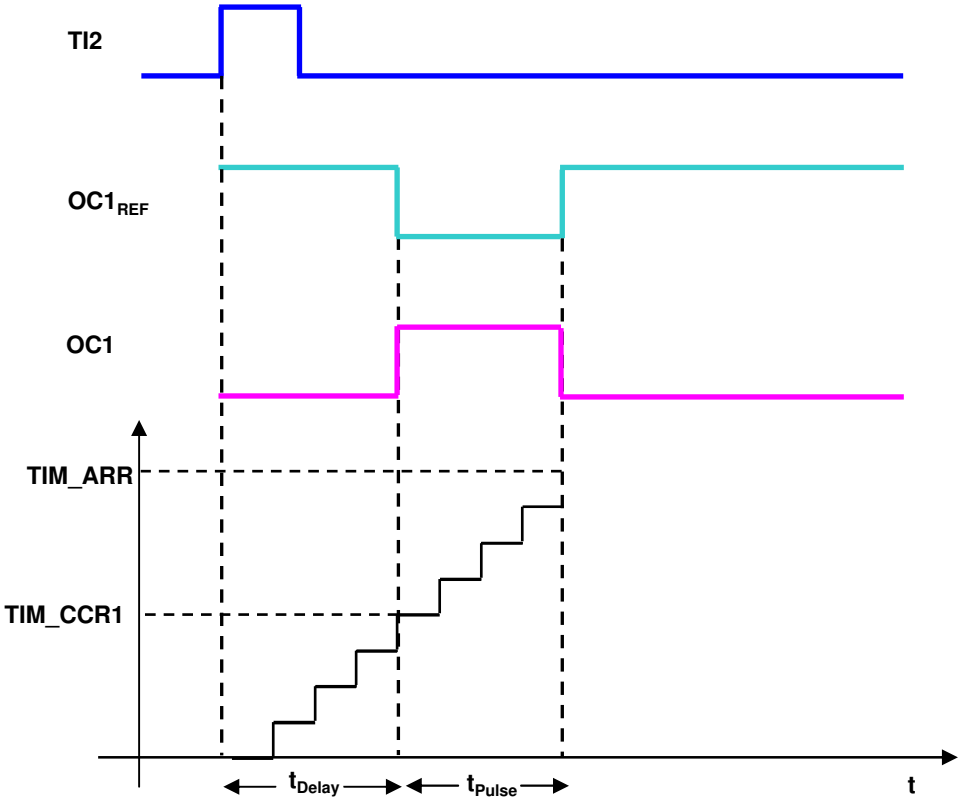
- IC1 or IC2 is selected as trigger input and the slave mode controller is configured in reset mode.



The PWM Input functionality enables the measurement of the period and the pulse width of an external waveform.

One Pulse Mode

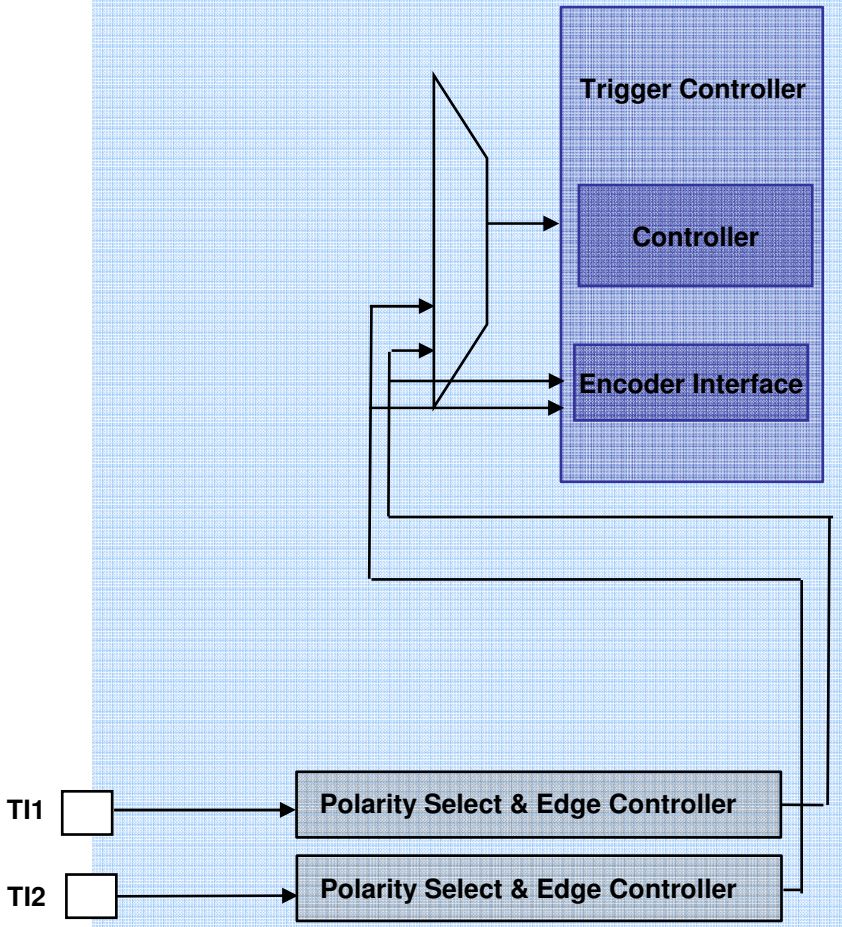
- One Pulse Mode (OPM) is a particular case of the previous modes: Ouput Compare and Input Capture.
- It allows the counter to be started in response to a stimulus and to generate a pulse with a programmable length after a programmable delay.
- There are two One Pulse Mode waveforms selectable by software:
  - Single Pulse
  - Repetitive Pulse



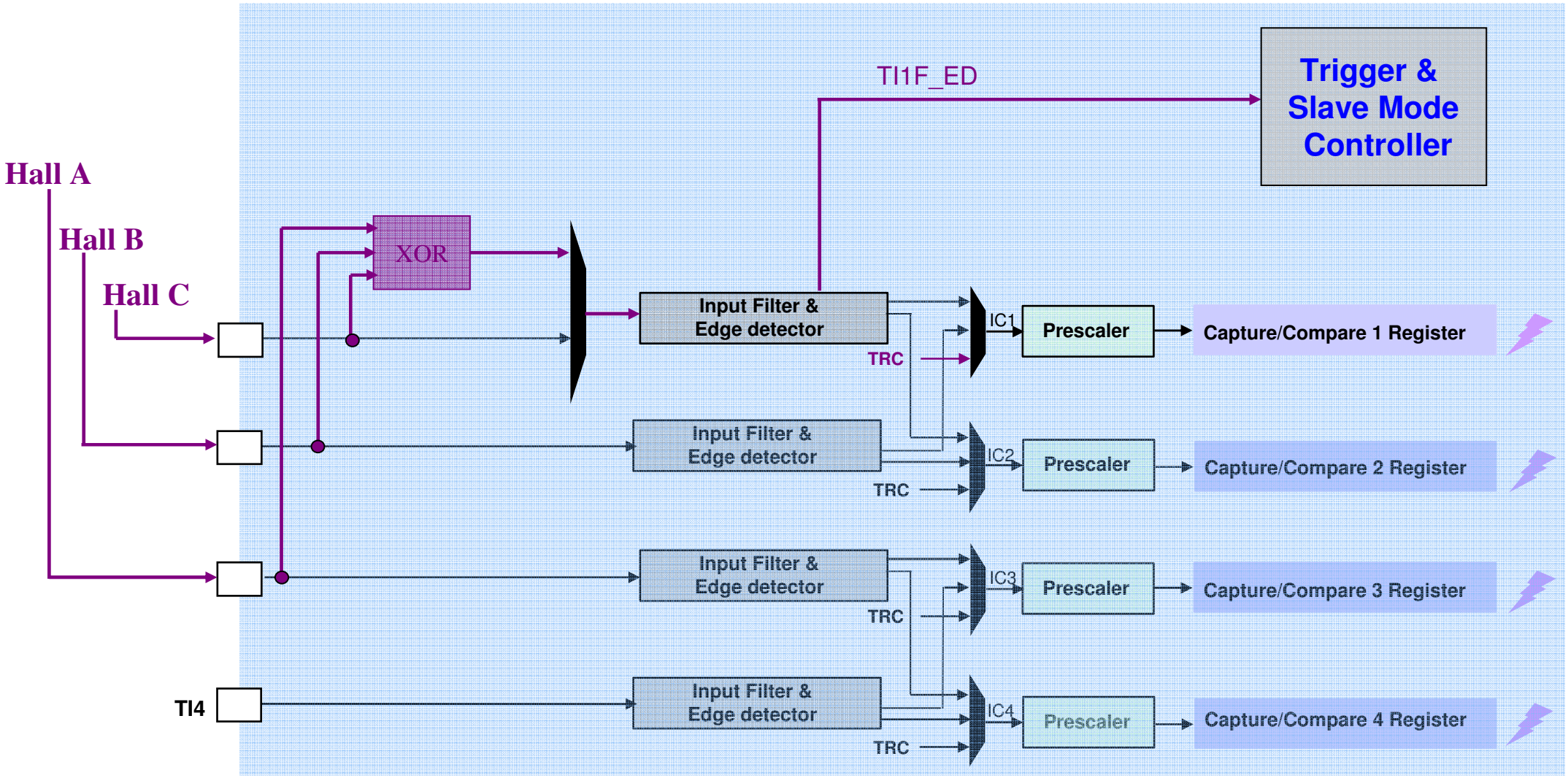
Encoder Interface

- Encoders are used to measure position and speed of motion systems (either linear or angular)
- The encoder interface mode acts as an external clock with direction selection
- The counter provides information on the current position (for instance angular position of an electric motor's rotor)
- To obtain dynamic information (speed, acceleration) on must measure the number of counts between two periodic events, generated by another timer
- Encoders and Microcontroller connection example:
  - An external incremental encoder can be connected directly to the MCU without external interface logic.

    The third encoder output which indicates the mechanical zero position, may be connected to an external interrupt and trigger a counter reset.

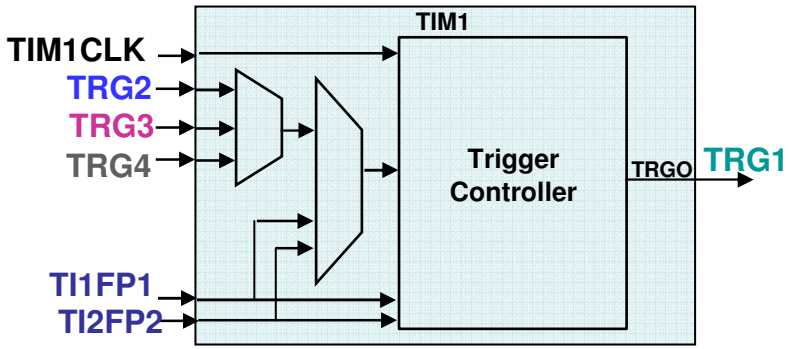


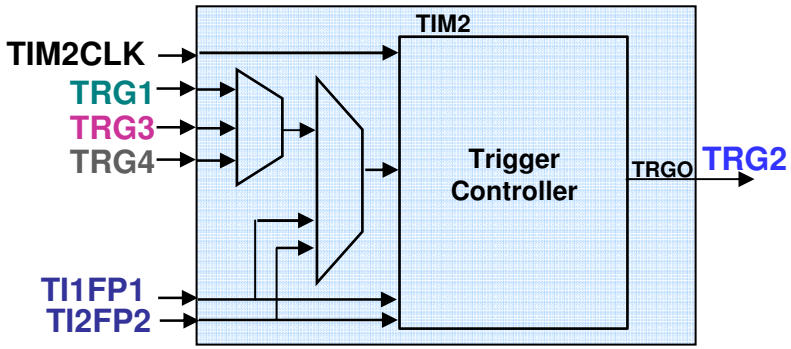
Hall sensor Interface

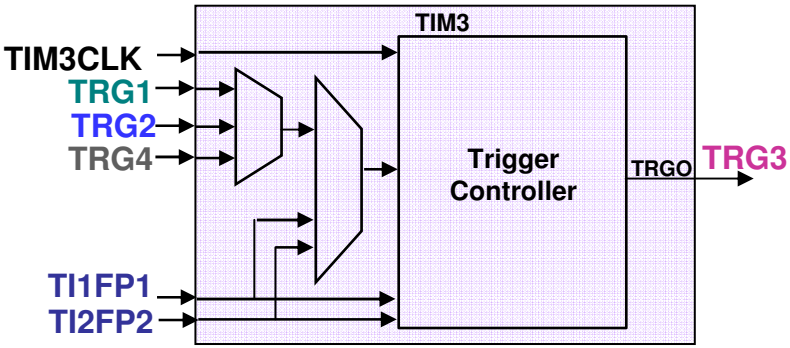


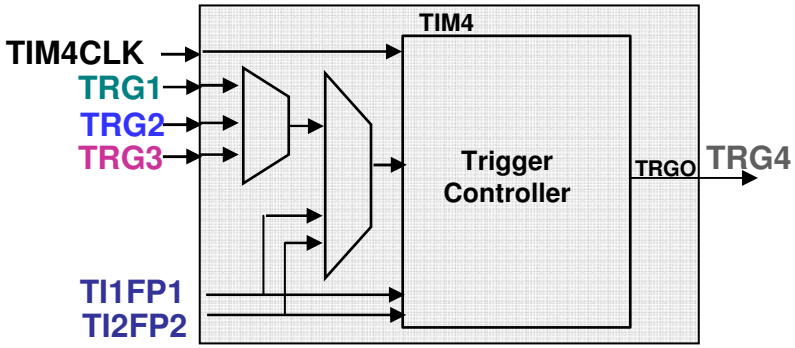
Timer Link System

- The four Timers are linked together for timer synchronization or chaining.



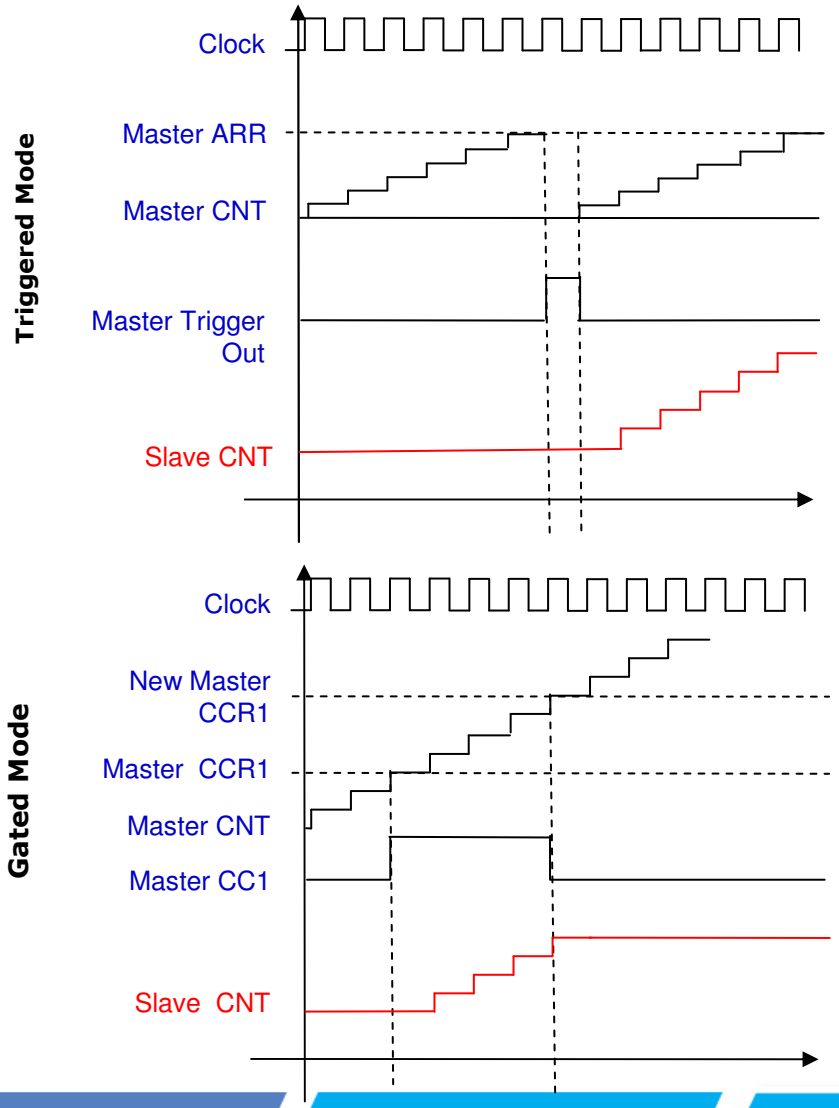






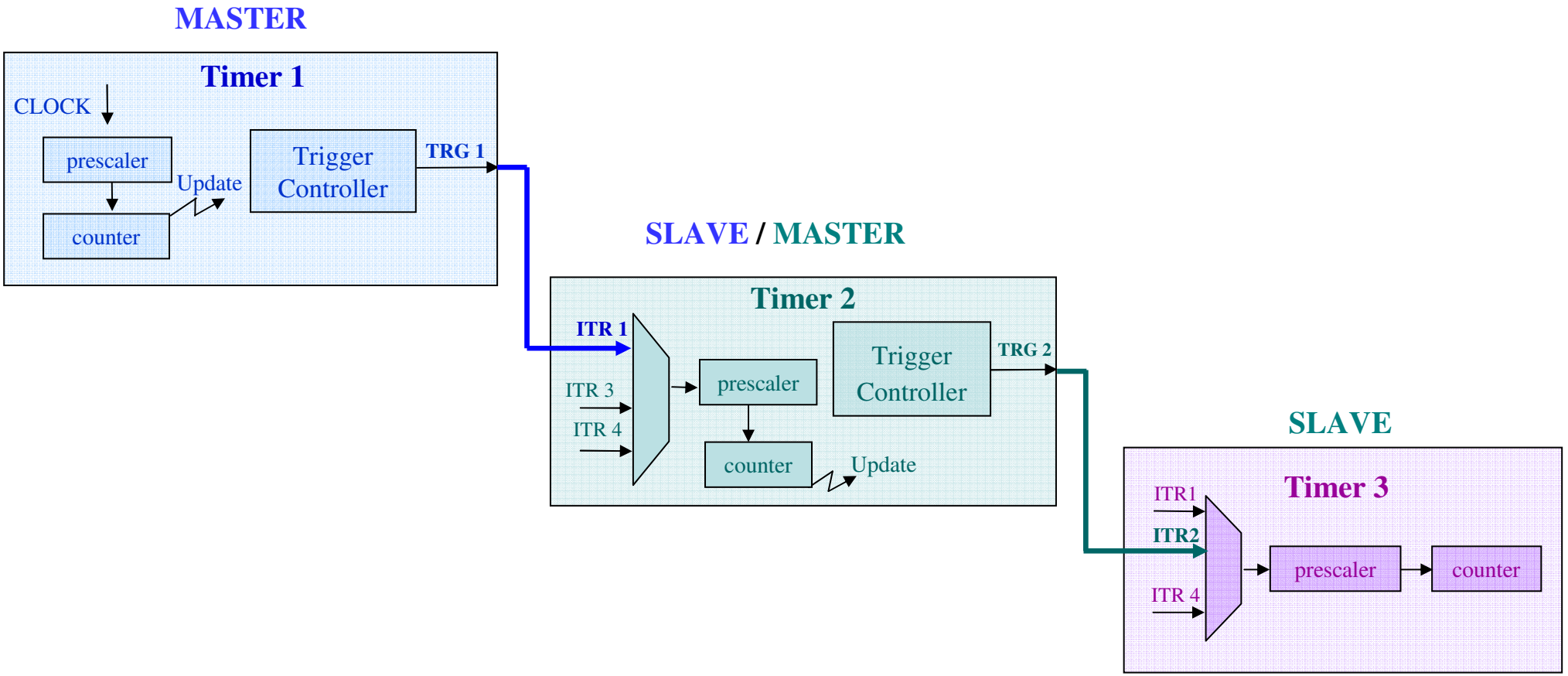
Synchronization Mode Configuration

- The Trigger Output can be controlled on:
  - Counter reset
  - Counter enable
  - Update event
  - OC1 / OC1Ref / OC2Ref / OC3Ref / OC4Ref signals
- The slave timer can be controlled in two modes:
  - Triggered mode : only the start of the counter is controlled.
  - Gated Mode: Both start and stop of the counter are controlled.



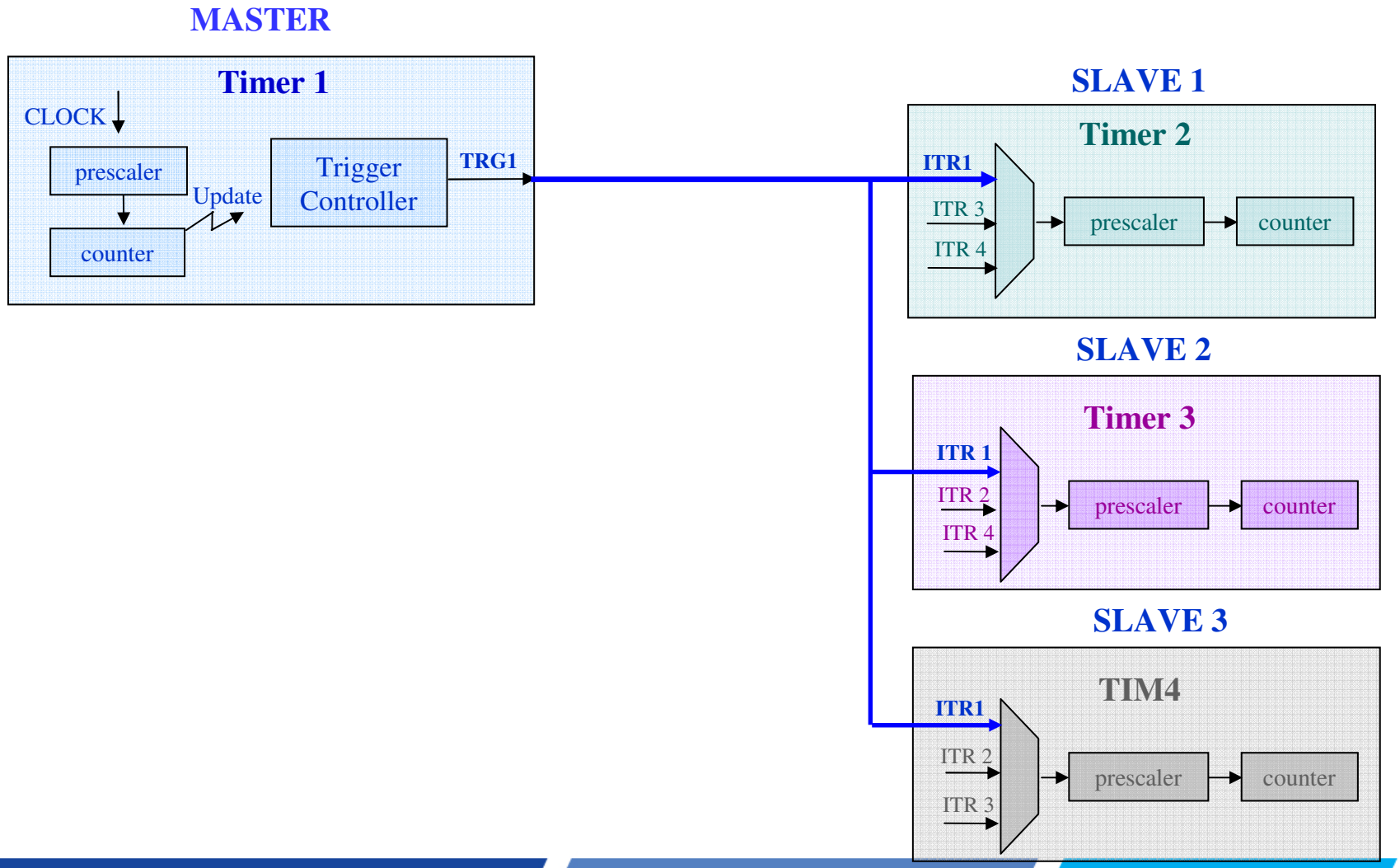
Synchronization – Configuration examples (1/3)

- Cascade mode:
  - TIM1 used as master timer for TIM2, TIM2 configured as TIM1 slave and master for TIM3.



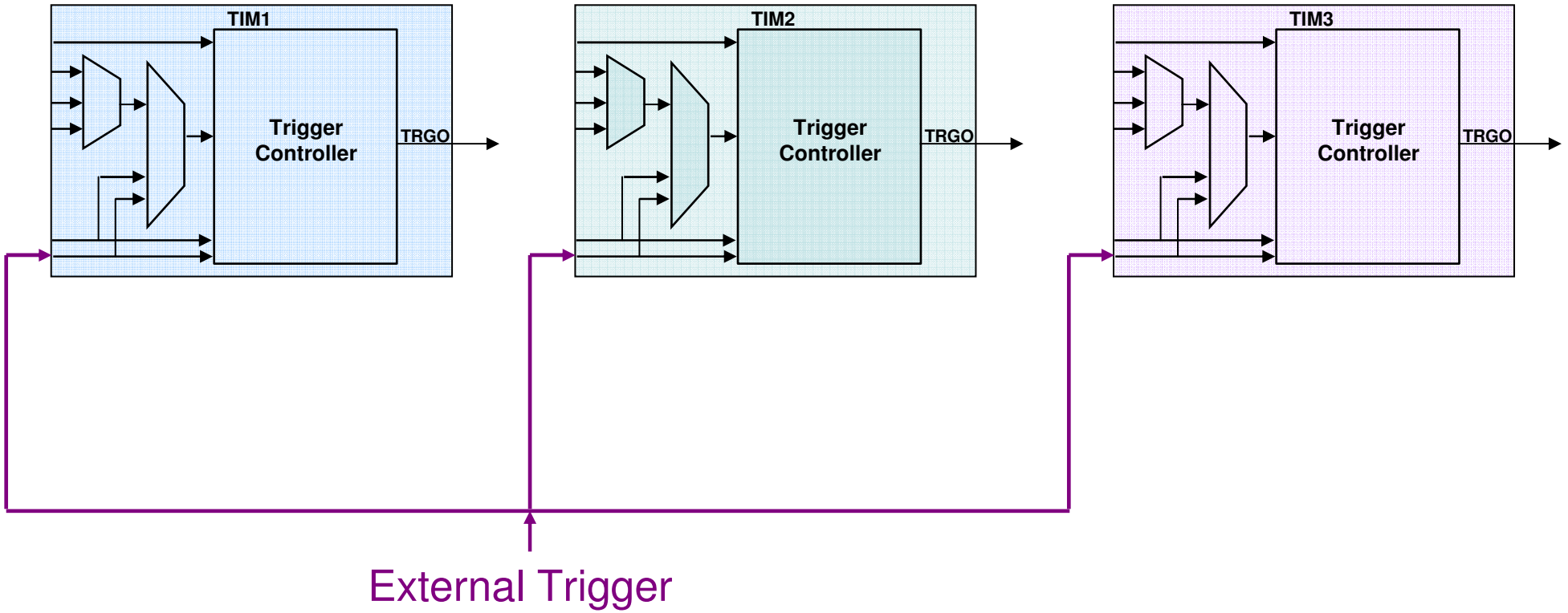
Synchronization – Configuration examples (2/3)

- One Master several slaves: TIM1 used as master for TIM2, TIM2 and TIM4.



Synchronization – Configuration examples (3/3)

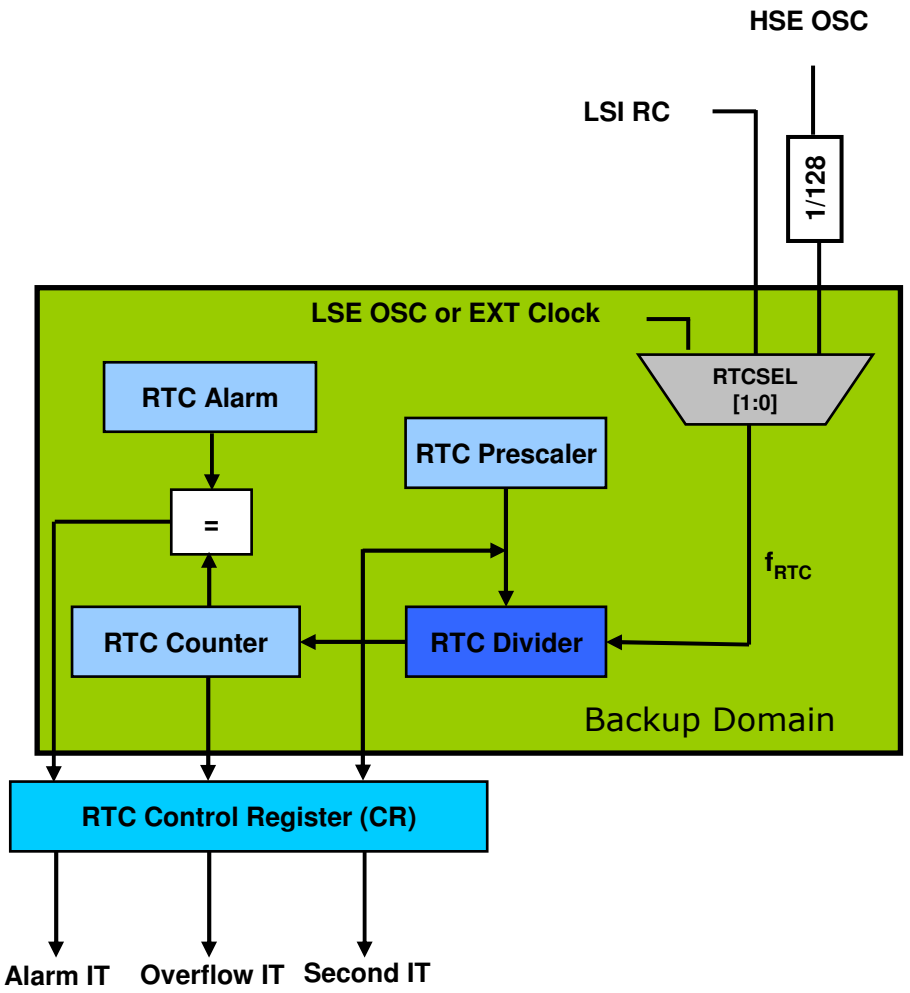
- Timers and external trigger synchronization
  - TIM1, TIM2 and TIM3 are slaves for an external signal connected to respective Timers inputs.



Other Timers

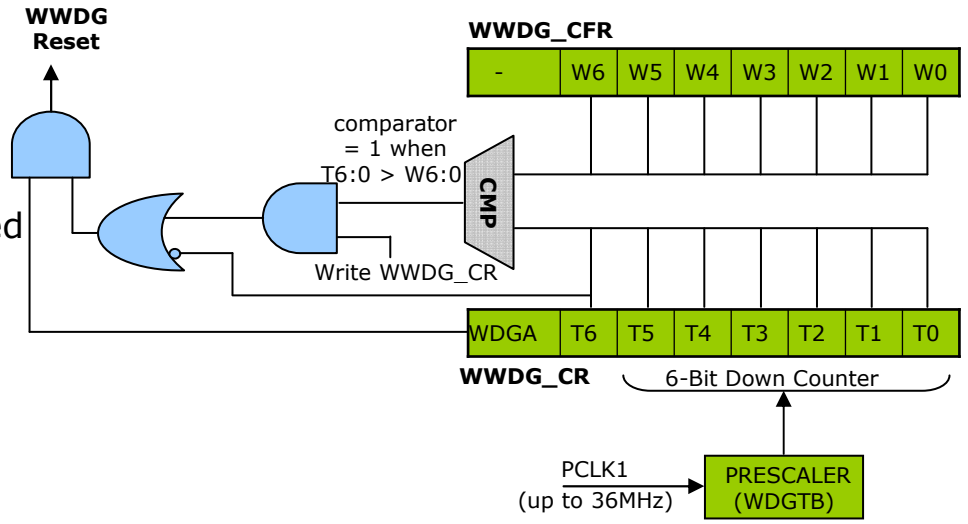
Real Time Clock (RTC)

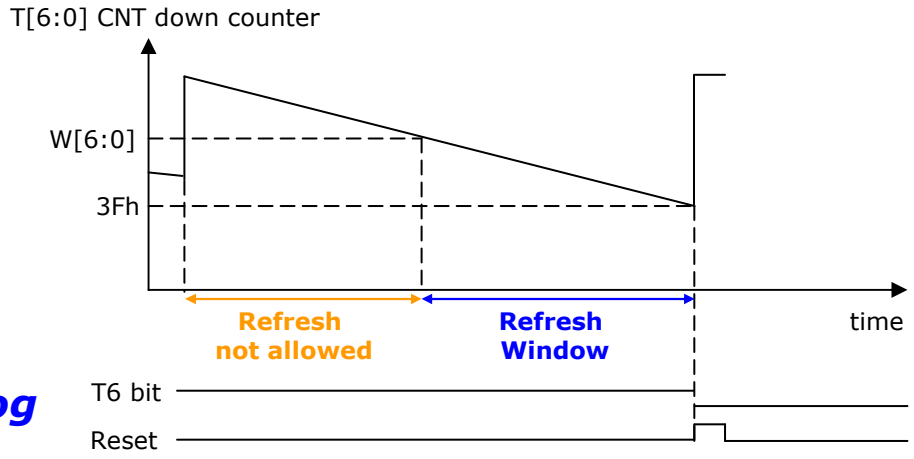
- **Clock sources**
  - 32.768 kHz dedicated oscillator (LSE)
  - Low frequency (32kHz), low power internal RC(LSI)
  - HSE divided by 128
- **3 Event/Interrupt sources**
  - Second
  - Overflow
  - Alarm (also connected to EXTI Line 17 for Auto Wake-Up from STOP)
- **Register protection against unwanted write operations**
- **RTC core & clock configuration in Backup domain**
  - Independent V_{BAT} voltage supply
  - Reset only by Backup domain reset
  - RTC config kept after reset or wake-up from STANDBY
- **Calibration Capability**
  - RTC clock can be output on Tamper pin for calibration
  - Then the clock can be adjusted from 0 to to 121ppm by a step of 1ppm



Window Watchdog (WWDG)

- Configurable time-window, can be programmed to detect abnormally late or early application behavior
- Conditional reset
  - Reset (if watchdog activated) when the down counter value becomes less than 40h (T6=0)
  - Reset (if watchdog activated) if the down counter is reloaded outside the time-window
- To prevent WWDG reset: write T[6:0] bits (with T6 equal to 1) at regular intervals while the counter value is lower than the time-window value (W[6:0])
- Early Wakeup Interrupt (EWI): occurs whenever the counter reaches 40h ➔ can be used to reload the down counter
- WWDG reset flag (in RCC_CSR) to inform when a WWDG reset occurs
- Min-max timeout value @36MHz (PCLK1): 113µs / 58.25ms

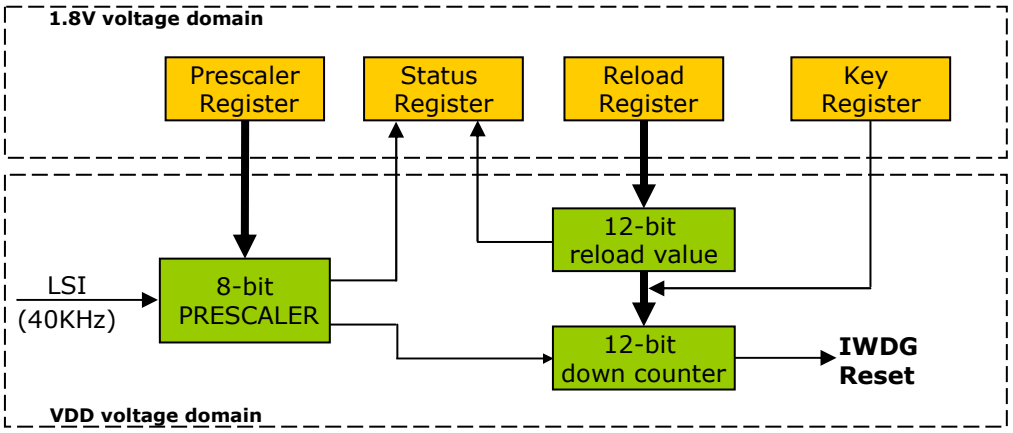




Best suited to applications which require the watchdog to react within an accurate timing window

IWDG features

- Selectable HW/SW start through option byte
- Advanced security features:
  - IWDG clocked by its own dedicated low-speed clock (LSI) and thus stays active even if the main clock fails
  - Once enabled the IWDG can't be disabled (LSI can't be disabled too)
  - Safe Reload Sequence (key)
  - IWDG function implemented in the VDD voltage domain that is still functional in STOP and STANDBY mode (IWDG reset can wake-up from STANDBY)
- To prevent IWDG reset: write IWDG_KR with AAAAh key value at regular intervals before the counter reaches 0
- IWDG reset flag (in RCC_CSR) to inform when a IWDG reset occurs
- Min-max timeout value @40KHz (LSI): 100µs / 26.2s



Best suited to applications which require the watchdog to run as a totally independent process outside the main application

System Timer (SysTick)

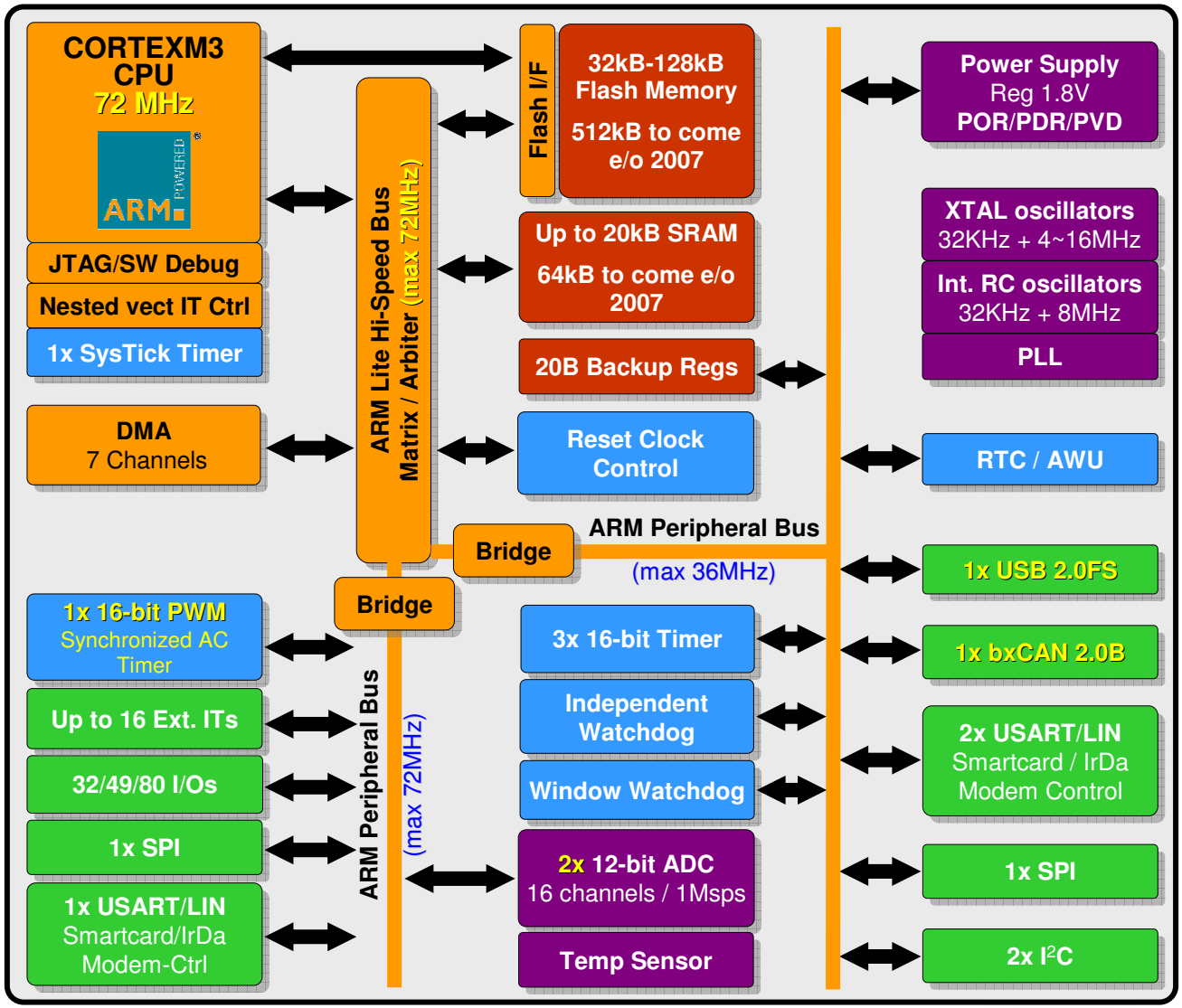
- Flexible system timer
- 24-bit self-reloading down counter with end of count interrupt generation
- 2 configurable Clock sources
- Suitable for Real Time OS or other scheduled tasks

In STM32F10x the SysTick clock can be: CPU clock or CPU clock/8 (provided externally by the Reset Clock Control)

Appendices

STM32F10x Series Block Diagram

- **ARM 32-bit Cortex-M3 CPU**
- **Nested Vectored Interrupt Controller (NVIC) w/ 43 maskable IT + 16 prog. priority levels**
- **Embedded Memories :**
  - FLASH: up 128 Kbytes, 512kB to come e/o 2007
  - SRAM: up 20 Kbytes, 64kB to come e/o 2007
- **7 Channels DMA**
- **Power Supply with internal regulator and low power modes :**
  - 2V to 3V6 supply
  - 4 Low Power Modes with Auto Wake-up
- **Integrated Power On Reset (POR)/Power Down Reset (PDR) + Programmable voltage detector (PVD)**
- **Backup domain w/ 20B reg**
- **Up to 72 MHz frequency managed & monitored by the Clock Control w/ Clock Security System**
- **Rich set of peripherals & IOs**
  - Embedded low power RTC with V_{BAT} capability
  - Dual Watchdog Architecture
  - 5 Timers w/ advanced control features (including Cortex SysTick)
  - 9 communications Interfaces
  - Up to 80 I/Os (100 pin package) w/ 16 external interrupts/event
  - Up to 2x12-bits 1Msps ADC w/ up to 16 channels and Embedded temperature sensor w/ +/-1.5° linearity with T°



STM32F10x Series Block Diagram

- **ARM 32-bit Cortex-M3 CPU**
- **Nested Vectored Interrupt Controller (NVIC) w/ 43 maskable IT + 16 prog. priority levels**
- **Embedded Memories :**
  - FLASH: up 128 Kbytes, 512kB to come e/o 2007
  - SRAM: up 20 Kbytes, 64kB to come e/o 2007
- **7 Channels DMA**
- **Power Supply with internal regulator and low power modes :**
  - 2V to 3V6 supply
  - 4 Low Power Modes with Auto Wake-up
- **Integrated Power On Reset (POR)/Power Down Reset (PDR) + Programmable voltage detector (PVD)**
- **Backup domain w/ 20B reg**
- **Up to 72 MHz frequency managed & monitored by the Clock Control w/ Clock Security System**
- **Rich set of peripherals & IOs**
  - Embedded low power RTC with V_{BAT} capability
  - Dual Watchdog Architecture
  - 5 Timers w/ advanced control features (including Cortex SysTick)
  - 9 communications Interfaces
  - Up to 80 I/Os (100 pin package) w/ 16 external interrupts/event
  - Up to 2x12-bits 1Msps ADC w/ up to 16 channels and Embedded temperature sensor w/ +/-1.5° linearity with T°